



20-24 April, Nice, France

Toshiba supports DATE with 'fabless' expert panel, technical papers and workshop session

Toshiba represented at Date '09 by European ASIC & Foundry business, Telecommunication Research Laboratory and Corporate R&D

Düsseldorf, Germany, 9 March 2009 - Toshiba Electronics Europe (TEE), Toshiba Research Europe Ltd (UK) and Toshiba Corporation (Japan) will all be actively supporting this year's DATE conference and exhibition. The TEE ASIC and Foundry business unit will be running one of the expert panel sessions and offering visitors the opportunity to pre-arrange private meetings with its team of specialists. Toshiba Research Europe's Telecommunications Research Laboratory will present a research paper, while experts from Toshiba Corporation's R&D facilities in Japan will present a paper and take part in a workshop.

Entitled 'Supporting fabless semiconductor design at 65nm and beyond', the TEE ASIC & Foundry panel session will be held on Wednesday 22nd April from 16:15 to 17:00 in the DATE exhibition theatre. The session will bring together representatives from a number of leading fabless manufacturers who will look at the process technologies available to chip designers targeting multimedia and communications applications. Differences between a traditional foundry model and an ASIC-orientated approach will also be considered. Among the topics that are likely to be debated are critical issues for future designs including technology cost, skills, risk of failure and system flow requirements in areas such as EDA, IP and external design support.

Panel members will be Rainer Kaese, the senior manager for SoC business development at Toshiba Electronics Europe; Jose Calero, CTO of DS2, a designer of powerline communication ICs; and Fernando Barbero, director of SoC development for TV module specialist SIDSA.

Pre-arranged meetings with Toshiba's ASIC & Foundry specialists will be held in meeting room Risso 7A. Here visitors will be able to discuss specific project requirements and find out more about Toshiba's advanced process technologies, business model and local support services. To see the TEE official DATE '09 invitation, and to find out more about the ASIC &

Foundry business, visit www.toshiba-components.com/ASIC. To arrange a meeting with ASIC & Foundry specialists during the exhibition e-mail date2009@tee.toshiba.de.

Toshiba's corporate R&D team will present a paper on 'Design and implementation of scalable transparent threads for multi-core media processors' at 17:00 on Wednesday 22nd April (<http://www.date-conference.com/conference/date09-session-8-8>). On Thursday 23rd April At 17:15 Toshiba Research Europe's Telecommunications Research Laboratory will present a paper entitled 'Implementation of a reduced lattice MIMO detector for OFDM systems' (<http://www.date-conference.com/conference/date09-session-12-3>). Finally, on Friday 24th April, Toshiba Corporation will look at 'Hierarchical cache system for 3D-multi-core processors in sub 90nm CMOS' as part of that day's workshop on W5 3D Integration (<http://www.date-conference.com/conference/date09-workshop-W5>).

The TEE ASIC & Foundry Business Unit's open and advanced Integrated Device Manufacturer (IDM) model allows customers to speed development and reduce risk by choosing a single partner for design, implementation, production and full-service supply chain management. The company offers a wide range of leading edge CMOS solutions based on Toshiba's own process developments. Customised SoC development is supported through a broad lineup of Intellectual Property (IP), including in-house and third party analogue and digital IP, ARM and MIPS processors, and embedded memory options.

To speed application development Toshiba offers local competence and support through its European LSI Design and Engineering Centre (ELDEC). ELDEC's highly skilled engineers have many years of experience in EDA, analogue development and design, implementation and layout. In addition, short development Turn-Around-Time (TAT) and low risk is assured thanks to flexible SoC design methodologies, optimised factory processes and professional project management.

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About Toshiba Electronics Europe

Toshiba Electronics Europe (TEE) is the European Headquarters for the electronic components business of Toshiba Corporation, which is the world's fourth largest semiconductor vendor according to estimates by Dataquest.

Providing design, manufacturing, marketing and sales, TEE was formed in 1973 in Neuss, Germany. The company now has headquarters in Düsseldorf, Germany and subsidiaries in France, Italy, Spain, Sweden and the United Kingdom. Company president is Mr. Hitoshi Otsuka and the total number of personnel in Europe is around 400.

Toshiba Electronics Europe offers one of the industry's broadest IC and discrete product lines including high-end memory, microcontrollers, ASICs, ASSPs and display products for automotive, multimedia, consumer, telecoms and networking applications. The company also has a wide range of power semiconductor solutions.

Toshiba Corporation is a leader in information and communications systems, electronic components, consumer products and power systems. The company's integration of these wide-ranging capabilities assures its position as an innovator in advanced components, products and systems. Toshiba operates a global network of more than 740 companies, with 198,000 employees worldwide and annual sales surpassing US\$76 billion.

For more company information visit Toshiba's web site at www.toshiba-components.com

About TRL

Since its inception in 1998, the Telecommunications Research Laboratory (TRL) has been at the cutting edge of research into technologies for next generation cellular, wireless local and personal area networks and reconfigurable device architectures. TRL works closely with colleagues in Toshiba's development laboratories to ensure a timely transfer of technology from its research phase, towards standardisation and into products.

For more information on TRL, visit: <http://www.toshiba-europe.com/research/trl/index.html>

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