

# TLP2116

- Plasma Display Panels (PDP)
- High-Speed Interfaces
- Factory Automation (FA)

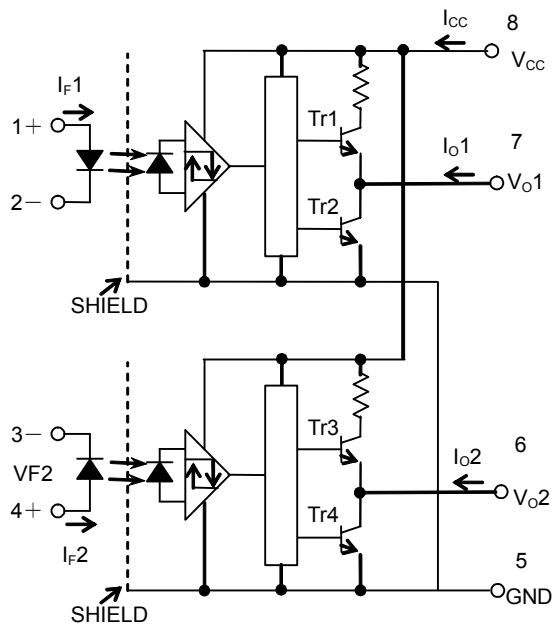
The TOSHIBA TLP2116 dual photocopler consists of a pair of GaAlAs light-emitting diodes optically coupled to integrated high gain and high-speed photodetectors.

- Inverter logic (totem-pole output)
- Package: SO-8
- Guaranteed performance over temperature : -40 to 100°C
- Power supply voltage: 4.5 to 5.5 V
- Input thresholds current:  $I_{FHL} = 5 \text{ mA (max)}$
- Propagation delay time (tpHL/tpLH): 75 ns (max)
- Switching speed: 15 MBd (typ.)(NRZ)
- Common mode transient immunity:  $\pm 10 \text{ kV}/\mu\text{s}$
- Isolation voltage: 2500 Vrms

**Truth Table**

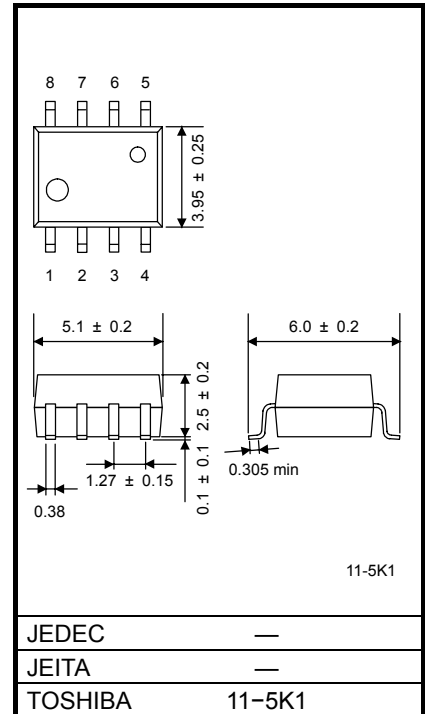
Input	LED1(2)	Tr1(3)	Tr2(4)	Output 1(2)
H	ON	OFF	ON	L
L	OFF	ON	OFF	H

**Schematic**



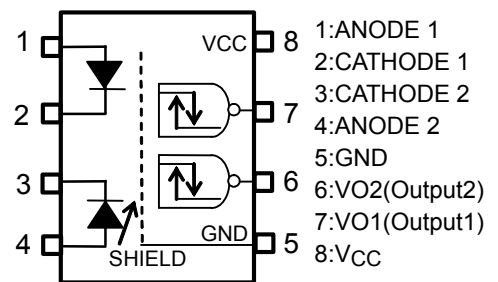
A bypass capacitor of 0.1  $\mu\text{F}$  must be connected between pins 8 and 5.

Unit: mm



Weight: 0.21g(Typ.)

**Pin Configuration (Top View)**



## Absolute Maximum Ratings (Ta=25°C)

Characteristic		Symbol	Rating	Unit
LED	Forward current (Each Channel)	$I_F$	20	mA
	Forward current derating (Ta ≥ 85°C) (Each Channel)	$\Delta I_F / \Delta T_a$	-0.5	mA/°C
	Peak transient forward current (Each Channel) (Note 2)	$I_{FPT}$	1	A
	Reverse voltage (Each Channel)	$V_R$	5	V
DETECTOR	Output current (Each Channel)	$I_O$	10	mA
	Output voltage (Each Channel)	$V_O$	6	V
	Supply voltage	$V_{CC}$	6	V
	Output power dissipation	$P_O$	40	mW
Operating temperature range		$T_{opr}$	-40 to 100	°C
Storage temperature range		$T_{stg}$	-55 to 125	°C
Lead solder temperature (10 s)		$T_{sol}$	260	°C
Isolation voltage (AC, 1min., R.H. ≤ 60%, Ta=25°C) (Note 2)		$BV_S$	2500	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pulse width  $PW \leq 1 \mu s$ , 300pps.

Note 2: This device is regarded as a two terminal device : pins 1, 2, 3 and 4 are shorted together, as are pins 5, 6, 7 and 8.

## Recommended Operating Conditions

Characteristic	Symbol	Min	Typ.	Max	Unit
Input current , ON (Each Channel)	$I_{F(ON)}$	8	—	18	mA
Input voltage , OFF (Each Channel)	$V_{F(OFF)}$	0	—	0.8	V
Supply voltage(*) (Note 3)	$V_{CC}$	4.5	5.0	5.5	V
Operating temperature	$T_{opr}$	-40	—	100	°C

(\*) This item denotes operating ranges, not meaning of recommended operating conditions.

Note 3: The detector of this product requires a power supply voltage ( $V_{CC}$ ) of 4.5 V or higher for stable operation.

If the  $V_{CC}$  is lower than this value, an  $I_{CCH}$  may increase, or an output may be unstable.

Be sure to use the product after checking the supply current, and the operation of a power-on/-off.

Note 4: A ceramic capacitor (0.1  $\mu F$ ) should be connected from pin 8 ( $V_{CC}$ ) to pin 5 (GND) to stabilize the operation of the high gain linear amplifier. Failure to provide the bypass may impair the switching property.

The total lead length between capacitor and coupler should not exceed 1 cm.

## Electrical Characteristics

(Unless otherwise specified, Ta=-40 to 100°C, VCC=4.5 to 5.5V)

Characteristic	Symbol	Conditions	Min	Typ.	Max	Unit
Input forward voltage (Each Channel)	V <sub>F</sub>	I <sub>F</sub> = 10 mA , Ta = 25°C	1.3	1.65	1.75	V
Temperature coefficient of forward voltage (Each Channel)	$\Delta V_F / \Delta T_a$	I <sub>F</sub> = 10 mA	—	-2.0	—	mV/°C
Input reverse current (Each Channel)	I <sub>R</sub>	V <sub>R</sub> = 5 V , Ta = 25°C	—	—	10	μA
Input capacitance (Each Channel)	C <sub>T</sub>	V = 0 , f = 1 MHz , Ta = 25°C	—	45	—	pF
Logic low output voltage (Each Channel)	V <sub>OL</sub>	I <sub>OL</sub> = 1.6 mA , I <sub>F</sub> = 12 mA, V <sub>CC</sub> = 5 V	—	—	0.4	V
Logic high output voltage (Each Channel)	V <sub>OH</sub>	I <sub>OH</sub> = -0.02 mA , V <sub>F</sub> = 1.05 V V <sub>CC</sub> = 5 V	4.0	—	—	V
Logic low supply current	I <sub>CCL</sub>	I <sub>F</sub> = 12 mA	—	—	10.0	mA
Logic high supply current	I <sub>CCH</sub>	V <sub>F</sub> = 0 V (Note 3)	—	—	10.0	mA
Input current logic low output (Each Channel)	I <sub>FHL</sub>	I <sub>O</sub> = 1.6 mA , V <sub>O</sub> < 0.4 V	—	—	5	mA
Input voltage logic high output (Each Channel)	V <sub>FLH</sub>	I <sub>O</sub> = -0.02 mA , V <sub>O</sub> > 4.0 V	0.8	—	—	V

\*All typical values are at Ta=25°C, V<sub>CC</sub>=5 V unless otherwise specified

## Isolation Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Conditions	Min	Typ.	Max	Unit
Capacitance input to output	C <sub>S</sub>	V <sub>S</sub> = 0, f = 1 MHz (Note 2)	—	0.8	—	pF
Isolation resistance	R <sub>S</sub>	R.H. ≤ 60%, V <sub>S</sub> = 500 V (Note 2)	1×10 <sup>12</sup>	10 <sup>14</sup>	—	Ω
Isolation voltage	B <sub>V</sub> <sub>S</sub>	AC, 1 minute	2500	—	—	V <sub>rms</sub>
		AC, 1 second, in oil	—	5000	—	
		DC, 1 minute, in oil	—	5000	—	V <sub>dc</sub>

## Switching Characteristics

(Unless otherwise specified, Ta=-40 to 100°C, VCC=4.5 to 5.5V)(Each Channel)

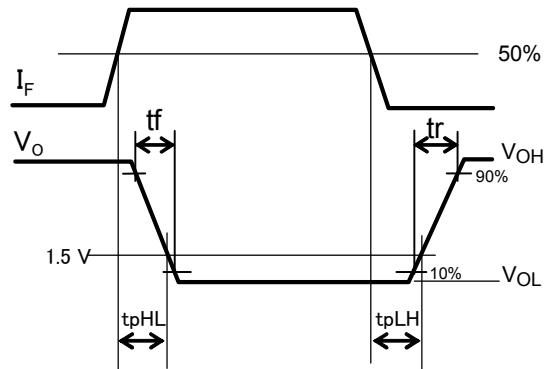
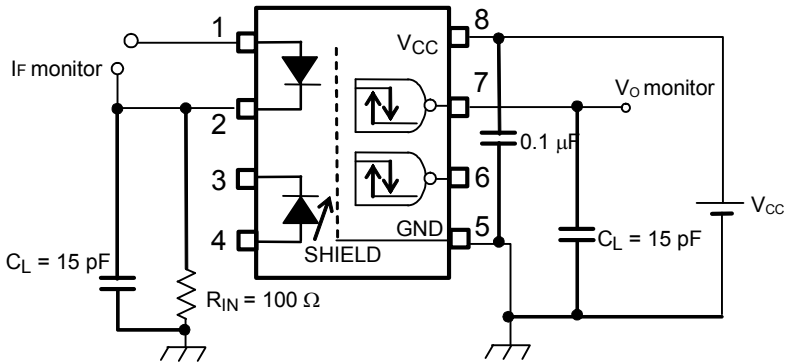
Characteristic	Symbol	Test Circuit	Conditions	Min	Typ.	Max	Unit	
Propagation delay time to logic low output	t <sub>pHL</sub>	1	I <sub>F</sub> = 0→12 mA	R <sub>IN</sub> = 100 Ω C <sub>L</sub> = 15 pF (Note 5)	—	—	75	ns
Propagation delay time to logic high output	t <sub>pLH</sub>		I <sub>F</sub> = 12→0 mA		—	—	75	ns
Propagation delay time to logic low output	t <sub>pHL</sub>	2	V <sub>IN</sub> = 0→5 V (I <sub>F</sub> = 0→8 mA)	R <sub>IN</sub> = 430 Ω C <sub>IN</sub> = 27 pF C <sub>L</sub> = 15 pF (Note 5)	—	—	75	ns
Propagation delay time to logic high output	t <sub>pLH</sub>		V <sub>IN</sub> = 5→0 V (I <sub>F</sub> = 8→0 mA)		—	—	75	ns
Switching time dispersion between ON and OFF	t <sub>pHL</sub> -t <sub>pLH</sub>	1	I <sub>F</sub> = 12 mA R <sub>IN</sub> = 100 Ω, C <sub>L</sub> = 15 pF (Note 5)		—	—	30	ns
Output fall time (90 - 10%)	t <sub>f</sub>		I <sub>F</sub> = 0→12 mA	R <sub>IN</sub> = 100 Ω	—	15	—	ns
Output rise time (10 - 90%)	t <sub>r</sub>		I <sub>F</sub> = 12→0 mA	C <sub>L</sub> = 15 pF (Note 5)	—	15	—	ns
Common mode transient immunity at high level output	CM <sub>H</sub>	3	V <sub>CM</sub> = 1000 Vp-p , I <sub>F</sub> = 0 mA, V <sub>O</sub> (min) = 4 V , Ta = 25°C		10000	—	—	V/μs
Common mode transient immunity at low level output	CM <sub>L</sub>		V <sub>CM</sub> = 1000 Vp-p , I <sub>F</sub> = 12 mA, V <sub>O</sub> (max) = 0.4 V , Ta = 25°C		-10000	—	—	V/μs

\*All typical values are at Ta=25°C

Note 5: CL is approximately 15 pF which includes probe and Jig/stray wiring capacitance.

## TEST CIRCUIT 1: Switching Time Test Circuit

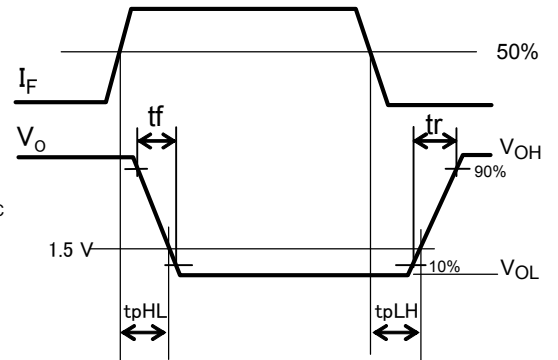
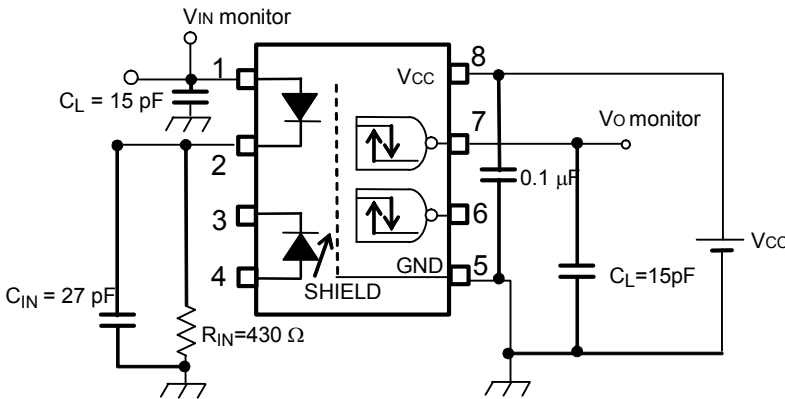
$I_F = 12 \text{ mA}$  (P.G)  
 ( $f = 5 \text{ MHz}$ , duty=50%,  
 less than  $t_r = t_f = 5 \text{ ns}$ )



$C_L$  is capacitance of the probe and JIG.  
 (P.G) : Pulse Generator

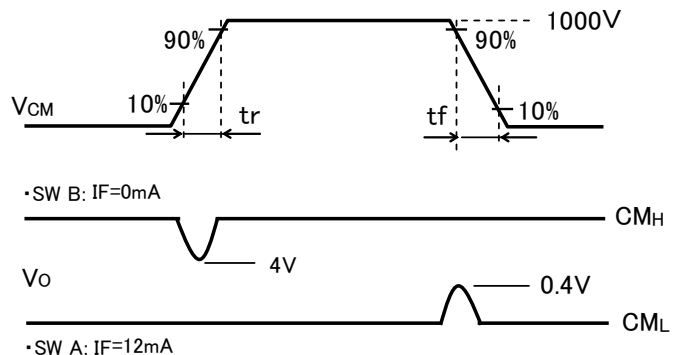
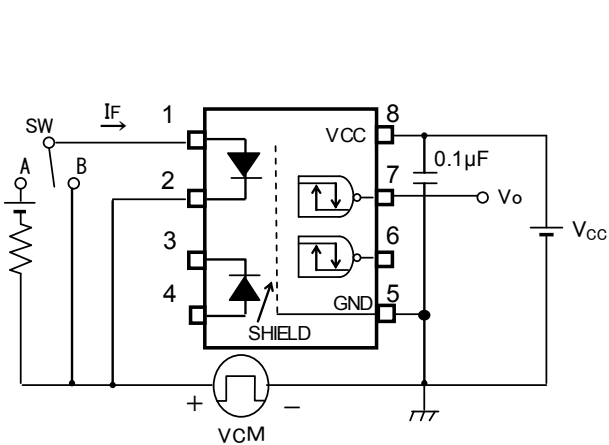
## TEST CIRCUIT 2: Switching Time Test Circuit

$V_{IN} = 5V$  (P.G)  
 ( $f = 5 \text{ MHz}$ , duty=50%,  
 less than  $t_r = t_f = 5 \text{ ns}$ )



$C_L$  is capacitance of the probe and JIG.  
 (P.G) : Pulse Generator

## TEST CIRCUIT 3: Common-Mode Transient Immunity Test Circuit



$$CM_H = \frac{800(V)}{t_r(\mu s)} \quad CML = -\frac{800(V)}{t_f(\mu s)}$$

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20070701-EN GENERAL

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