

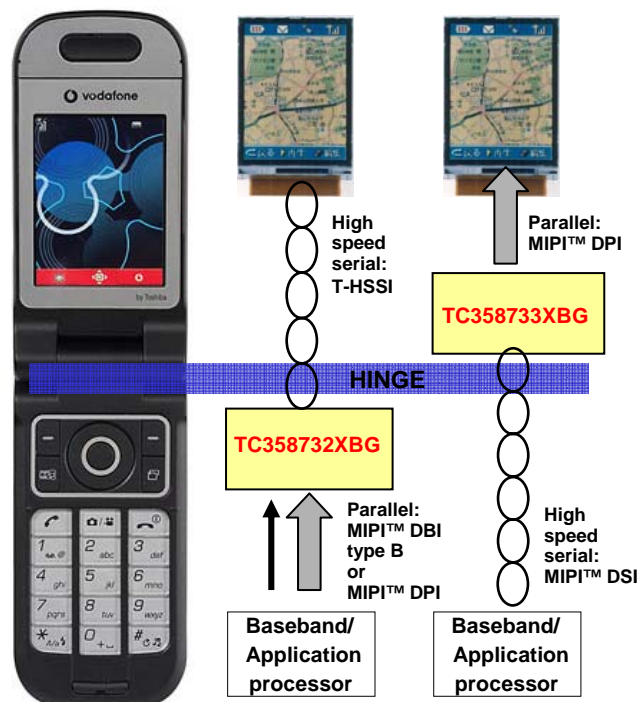
enhanced MIPI™ Display Controller

Overview

TC358731/2/3XBG

Toshiba's enhanced Display Controller devices TC358731/32/33XBG are developed to reduce the total system power consumption when large size mobile displays have to be driven. The embedded image buffer enables the connection of displays up to VGA resolution and offloads some performance hungry display tasks from the host CPU. TC358731/32/33XBG will buffer the display content from the host and updates the connected LCD with the required timing and frame rate.

TC358731/32/33XBG supports a variety of different host and display interfaces. This makes the product applicable for a wide range of existing and upcoming baseband and application processors. As TC358731XBG supports high speed serial connections for the host as well as for the display interface, it is very applicable for all different phone types like candy bar, slider, clam shell or twister phones



Application / Benefits

- Reduction of overall system power consumption
 - Real time update of the connected LCD mode with the required frame rate while the host can sleep
 - High speed burst access from the host
- Flexible image buffer handling
 - Single buffer for images of maximum VGA size
 - Automatic double buffering for images of maximum HVGA size
- Easy adoption of different LCD module orientations by rotation and mirroring of incoming image
- Support for 16, 18 and 24 bit RGB data for input and output images together with color depth conversion option
- Improvement of image quality by Toshiba original Magic Square™ algorithm
- Flexible and future proof interfaces towards the baseband
 - Enabled for existing baseband architectures with MIPI™ DBI-type B, MIPI™ DPI
 - Equipped for upcoming processor generation with a high speed serial MIPI™ DSI interface (TC358731/33XBG only)
- Flexible interfaces towards the display module
 - High speed serial interface T-HSSI
 - Parallel, MIPI™ DPI compliant interface (TC358731/33XBG only)

Product Features

Low power features:

- Support for Sleep and Deep Sleep modes
- High speed burst access enables longer sleep times of the baseband processor
- Low power 8Mbit embedded DRAM frame buffer included on chip
- Low leakage process technology

Three different interface standards to the baseband

- MIPI™ DBI type B with 8 and 16 bit bus width for command and video data
- MIPI™ DPI with 8 and 12 bit bus width for video data plus MIPI™ DBI type C for command data
- High speed serial MIPI™ DSI interface for command and video data (TC358731/33XBG)

Two different interface standards to the LCD:

- MIPI™ DPI with 18 bit bus width (TC358731XBG) and 24 bit bus width (TC358733XBG)
- High speed serial T-HSSI with 2 data channels (TC358731/32)

Flexible image buffer handling:

- Single buffer usage for images with flexible width and height of maximum VGA size
- Double buffer usage for two images of maximum HVGA size with automatic buffer swapping

MIPI™ DCS compliant software interface

Enables easy software integration

Image processing capabilities

- Rotation of incoming images
- Mirroring of incoming and outgoing images
- Quadruple mode to double incoming pixels in horizontal and vertical orientation
- Bit depth conversion from incoming to outgoing image
- Image quality enhancement by Toshiba original Magic Square™ algorithm

PWM output

- Enables flexible backlight control

MIPI™ DBI type C output

- MIPI DBI type C to configure the connected LCD module

System clock:

- Support for a low speed 32 kHz input clock or
- Support for a high speed input clock of flexible frequency

Voltage supply

- Core and IO: 1.8V ; add. 1.2V&2.5V (TC358731/33XBG)

Package:

- P-VFBGA64-0505-0.50
- 64 pin 0.5 mm ball pitch package
- maximum height 1.0 mm, 5x5 mm²

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