



Cheaper options for chip designs

Published on 20 July 2009



How can you get chips onto the market when you don't have an iPhone budget?

Since the late 1990s, people have complained bitterly about the rapidly rising cost of non-recurrent engineering (NRE) charges on chip designs and what would quickly become the biggest component of those charges: the amount of money needed to make a full set of layout masks. In little more than ten years, the price for a mask set went from tens of thousands of dollars through hundreds of thousands and now sits in the low millions.

However, when you take into account the software and hardware design and verification costs, even the amount of cash needed for a mask becomes practically insignificant. And then you have the problem of companies from different markets converging on a shrinking number of positions on the printed circuit board (PCB). You have to bet big and win big to not be faced with the situation of watching money go down the drain. It's a situation that has frightened venture capital companies away and made many in the industry wonder how new chip startups can get anywhere near enough funding to get to market.

As an integrated device manufacturer (IDM), Toshiba has made application-specific integrated circuits (ASICs) for customers for several decades but it is an industry in decline. At the recent GSA and IET International Semiconductor Forum, ...

Tatsuo Noguchi, technology executive for Toshiba, reckons: "Advanced processes, such as 65nm, carry a high risk of failure. Even more challenges and risks are coming to the fore. At 28nm, to go from concept to production will take more than \$100m. Can any venture capital firm cover this? And, if yes, who can?"

"The majority of fabless companies will definitely require a new model. The COT model can only be used by companies with huge operational teams. The majority will need a new model."

Fabless dilemma

Noguchi sees the COT model as being too burdensome even for those in the ASSP business to bear. "The fabless ASSP companies' core competencies are the architecture and functionality of their SoC products. But they are forced to use the COT model," he says. "They need to establish or outsource test and assembly, which carries risk, and invest in libraries and tools and a place-and-route infrastructure. But there is no differentiator in these functions."

Toshiba's plans to offer flows that are modelled on the traditional ASIC and COT approaches but provide options that let fabless companies use libraries and cores designed or migrated by the Japanese chipmaker to its processes. Companies opting for a more ASIC-like engagement will be able to provide their own IP blocks that will be incorporated into a chip by a Toshiba design centre at the place-and-route stage. Customers will hand off either RTL code or a netlist, with place-and-route performed by Toshiba. "The customer doesn't have to invest the EDA environment," says Noguchi.

With the hybrid models, the Toshiba offering will put the Japanese company into more direct competition with specialist design and operational support firms such as eSilicon, which use external foundries for manufacturing. Jack Harding, president and CEO of eSilicon, says moves such as Toshiba's reflect a need to use up fab capacity.

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Reprint courtesy of The IET → <http://kn.theiet.org/magazine/issues/0913/cheaper-chip-designs-0913.cfm>