

ASIC & Foundry

eFUSE - Electrical Programmable Fuse One-Time-Programmable (OTP) Memory Macro

A flexible, cost efficient and easy-to-use solution for System-on-Chip (SoC) Integration

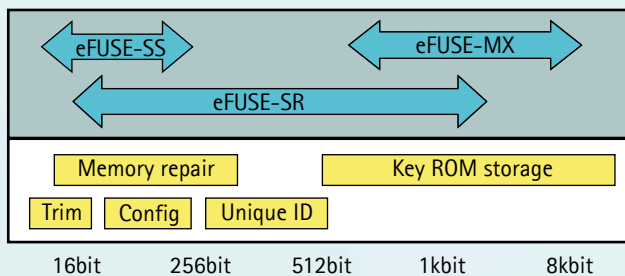
Toshiba complements its technology, library and IP lineup for ASIC and COT/Foundry with an attractive OTP memory solution: "eFUSE" is a macro that contains electrically programmable fuses (PMOS gate oxide anti-fuses). The eFUSE macro is available in all SoC technologies and can be implemented in a standard CMOS process without any need for additional process options.

eFUSE is provided as a fully integrated OTP macro with customer-selected configurations. Read operation requires only standard core voltage supply and the programming voltage for write operation is internally generated (out of a 3.3V supply).

eFUSE Applications

eFUSE is the optimal solution for many applications such as:

- Configuration/Version data
- Trimming data
- Identification and tracing ("Chip-ID")
- Embedded RAM redundancy (auto-repair) data
- Key ROM storage for secure data transmissions



eFUSE Lineup

eFUSE Line-up	130nm	90nm	65nm	40nm
General Purpose	eFUSE-SR (64bit to 1kbit)	eFUSE-SR (64bit to 1kbit)	eFUSE-SR (64bit to 1kbit)	
High Capacity			eFUSE-MX (1Kbit to 8kbit)	eFUSE-MX (1Kbit to 8kbit)
Small Cap (Trim/ID)				eFUSE-SS (16bit)

Three types of eFUSE macros are available. The generic eFUSE-SR offers a capacity of 64bit to 1kbit in increments of 64bit, with serial access.

For 65nm technology, a high capacity solution called eFUSE-MX with random access is added, with up to 8Kbit capacity.

For 40nm an additional small capacity macro of 16bits of Poly-fuse is added to the lineup.

eFUSE Support

Programming of eFUSE can be done by the customer or end-user (at manufacturing, in-field, in-operation), but also by Toshiba as a programming service during the test-phase. Customers can specify memory content or provide algorithms to generate the content.

As for design support, models for all major EDA platforms, datasheets, applications notes and implementation guidelines are available through the local Toshiba ASIC/Foundry support teams.

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