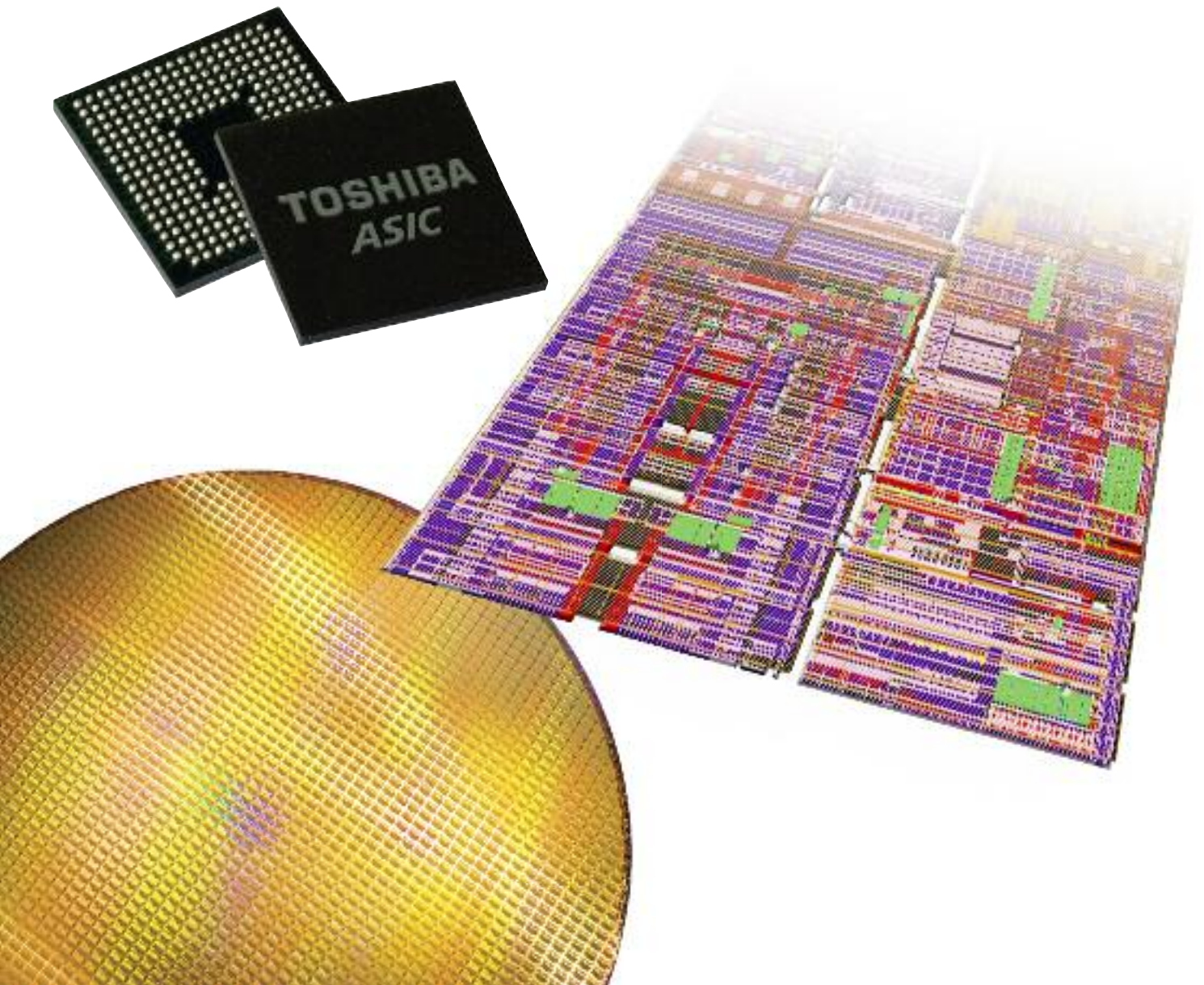


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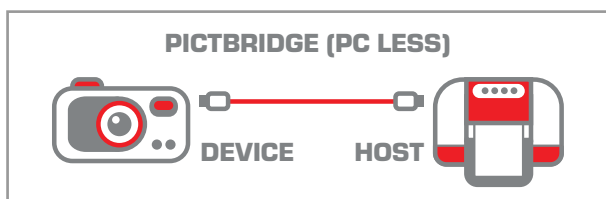
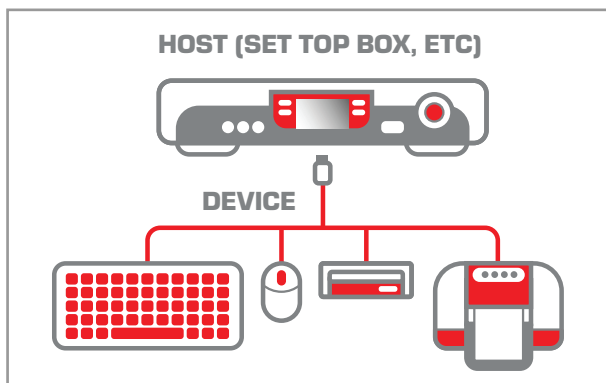
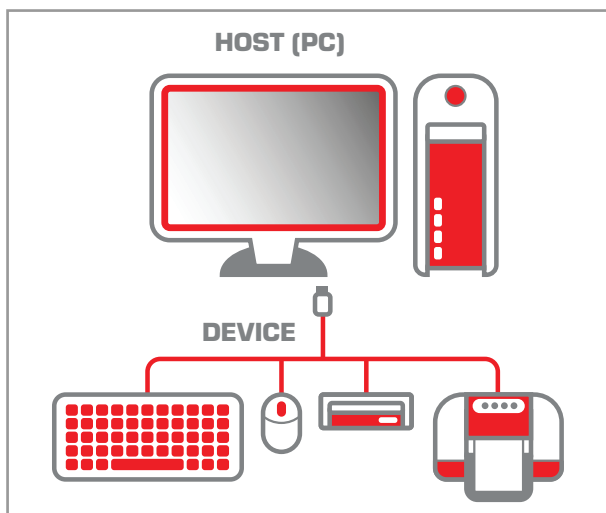
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- > **ASIC & FOUNDRY SOLUTIONS FOR USB**
- > **USB 2.0 PHY IP**
- > **MIXED SIGNAL IP**



> USB SYSTEM

The Universal Serial Bus (USB) has become well-established for the interconnection of a wide variety of peripherals and other equipment designed to communicate with a host desktop or laptop PC. USB can also increasingly be found as a connectivity option in 'convergent' consumer electronics products such as set top boxes, while USB 'On-the-Go' (OTG) provides 'PC-less' connectivity between portable products by providing limited host capability to communicate with selected USB-enabled peripherals.



Operating at speeds of up to 480Mbps/s, USB 2.0 - or Hi-Speed USB - supports the connectivity requirements of increasingly sophisticated peripheral products and portable devices that need to transmit and receive high volumes of data.

> TOSHIBA'S USB 2.0 PHY IP

Toshiba's USB 2.0 PHY is an IP block that provides an advanced, flexible and future-proofed solution for system designers looking to quickly and easily integrate USB functionality into a system-on-chip (SoC) ASIC. The PHY provides physical layer functionality for USB 2.0 and is used as the interface between the USB Host or Device Controller and the USB system.



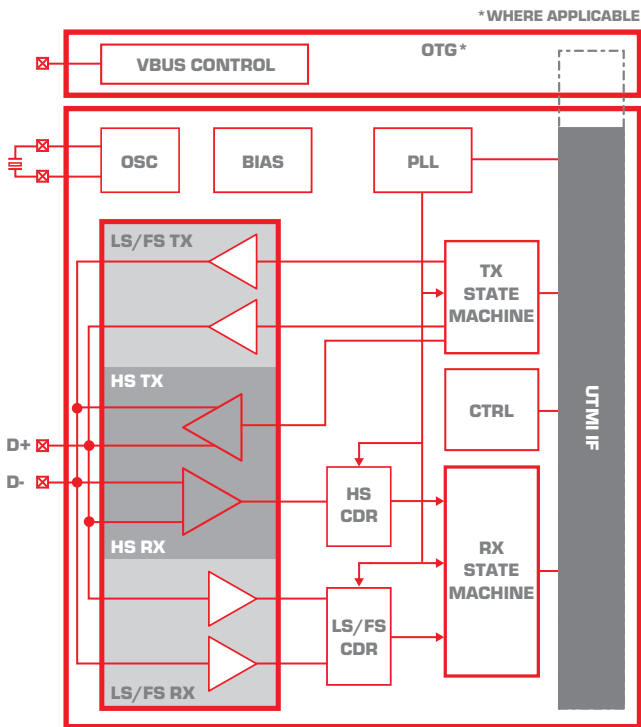
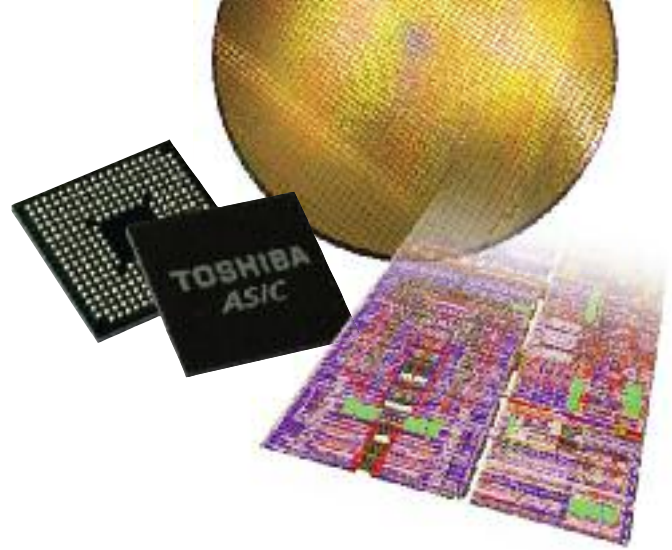
Toshiba's USB 2.0 PHY processes the USB protocol and physical layer signalling. The PHY supports SYNC detection, parallel-to-serial and serial-to-parallel data conversion and data recovery.

The PHY port has three different external interfaces as follows:

- > **USB Data+ (DP) Data- (DM) lines**
These lines are compliant to the USB 2.0 specification and support Hi-Speed (HS) 480Mbps transmission. The PHY also supports USB 1.1 Full-Speed (FS) transmission at 12Mbps and Low-Speed (LS) transmission at 1.5Mbps.
- > **Interface with Host Controller or Device Controller**
The reception port and transmission port provide 16-bit parallel communication in HS and FS modes
Toshiba's USB 2.0 Link Host Controllers are available with PCI or AHB interface options
- > **Serial interface (only used for Host applications)**
The transmission/reception interface with this controller supports FS and LS communication

The PHY has the following features:

FEATURES AND BENEFITS
USB 2.0 specification compliance
UTMI+L3 interface
Integrated 45Ω termination resistors, 1.5kΩ pull-up resistors, 15kΩ pull-down resistors
480Mbps (HS), 12Mbps (FS), 1.5Mbps (LS) transmission rates
Supports serial data recovery function on USB
Supports SYNC/End-of-Packet (EOP) and check functions
Supports bit stuffing, bit unstuffing and bit stuffing error detection functions
Supports Non Return to Zero Invert (NRZI) encoding and decoding functions
Supports parallel-to-serial and serial-to-parallel data conversion
Supports Suspend and Resume functions
Supports the USB 2.0 test mode
Generates a 480MHz clock for HS operation using an integrated PLL
Can use a 12MHz crystal oscillator or 12MHz external clock as a reference clock source
Supports tuning functions to optimise analogue characteristics
Supports VBUS Detection Circuit

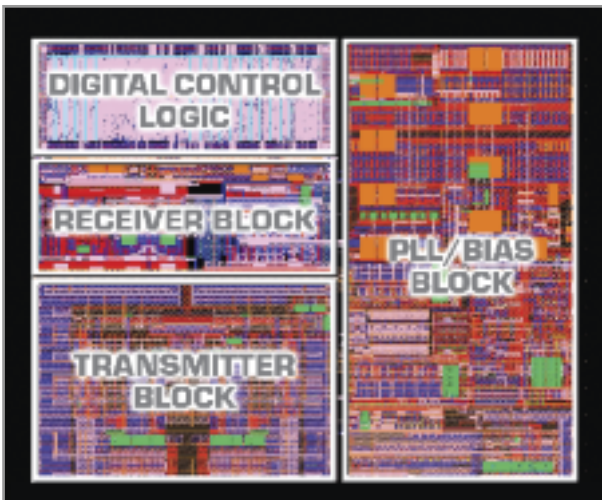


Toshiba's USB2.0 comprises the following blocks:
 The transceiver module, a common PLL/bias block, the digital control logic, and OTG functionality*.
 *For 90/65/40nm technology

The Common block includes an internal clock generator for accurate HS data transmission. The integrated PLL can operate either from an external crystal or an internal clock source. All required reference currents and voltages are generated in this block.

The transceiver module offers the USB2.0 compliant serial data transmission and reception including data recovery for HS, FS and LS signalling.

Data processing including serializer/deserializer bit stuffing etc. is performed in the digital control block. This block supports ATE and provides a UTM I+L3 compliant interface.



The OTG block contains the prerequisites for realizing the USB-OTG functionality that allows for PC-less communication between products.

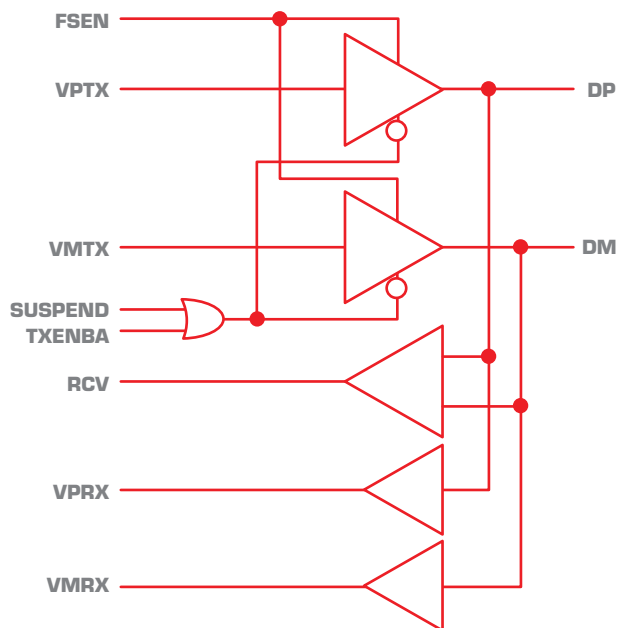
Fully silicon-proven, Toshiba's USB 2.0 PHY is available for seamless integration in following advanced CMOS processes:

- > TC340 40nm 1.0V process
- > TC320 65nm 1.2V process
- > TC300 90nm 1.2V process
- > TC280 130nm 1.5V process (without OTG functionality)

The IP is supplied as a mixed-signal hard macro and GDSII, abstracts, models for major EDA tools and detailed application notes are all available.

> TOSHIBA'S USB 1.1 SOLUTION

For Full Speed (FS) and Low Speed (LS) serial data transmission, Toshiba also offers an optimized USB1.1 I/O solution which complies with the Universal Serial Bus specification rev.1.1.

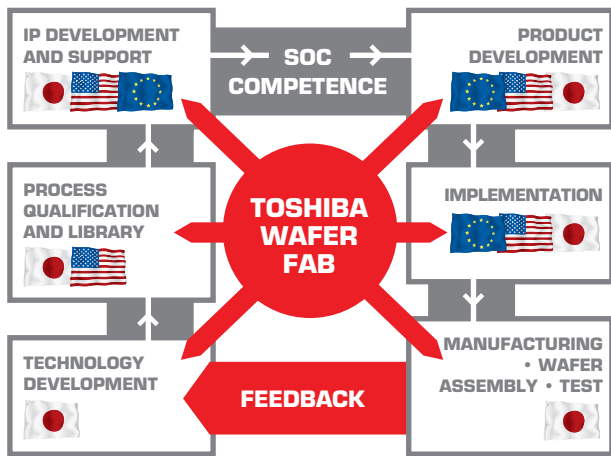


Toshiba's USB1.1 I/O is silicon-proven and ready for integration in the following CMOS processes:

- > TC340 40nm 1.0V process (under planning)
- > TC320 65nm 1.2V process
- > TC300 90nm 1.2V process
- > TC280 130nm 1.5V process
- > TC260 180nm 1.5V process

> THE IDM MODEL

The IDM model means that all of the hard macro IP cores developed by Toshiba's engineering teams are guaranteed to be fully compatible and optimised for the company's advanced SoC processes. This guarantee also applies to third party architecture-based IPs provided through the Toshiba channel, which are subject to exactly the same rigorous qualification and verification procedures.



As an IDM, Toshiba's intimate involvement with the underlying process technology and rapid access to production feedback ensures that designs can be optimised and customised with final production in mind from the very beginning of the development process. This includes verifying and testing of IP in the customer product.

For the customer, the IDM model also eliminates the blurring of the boundaries of responsibility. Toshiba's responsibility encompasses everything from IP to final production and yield optimisation, providing the peace of mind that customers are working with a company that shares their objective of delivering successful volume silicon with the shortest possible turn-around-time (TAT).

> SUPPORTING SOC IMPLEMENTATION

To speed and simplify the implementation of SoCs based on the company's advanced CMOS processes, Toshiba offers a variety of development handover models including:

- > ASIC model
- > RTL handover with synthesis, place-and-route, and verification by Toshiba or gate-level handover with synthesis by customer and layout implementation by Toshiba Seamless "hybrid" models
- > Mixed-signal IP/block development by customer based on PDK, and chip-level integration by Toshiba (RTL handover or gate-level handover)
- > Full COT (customer own tooling) model, with physical data handover (GDSII) by customer.

In each handover model, engineers at Toshiba's local European LSI Design and Engineering Center (ELDEC) are available to provide full technical support, advice and guidance relating to the integration-, QA- and testing of the USB IP.

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