

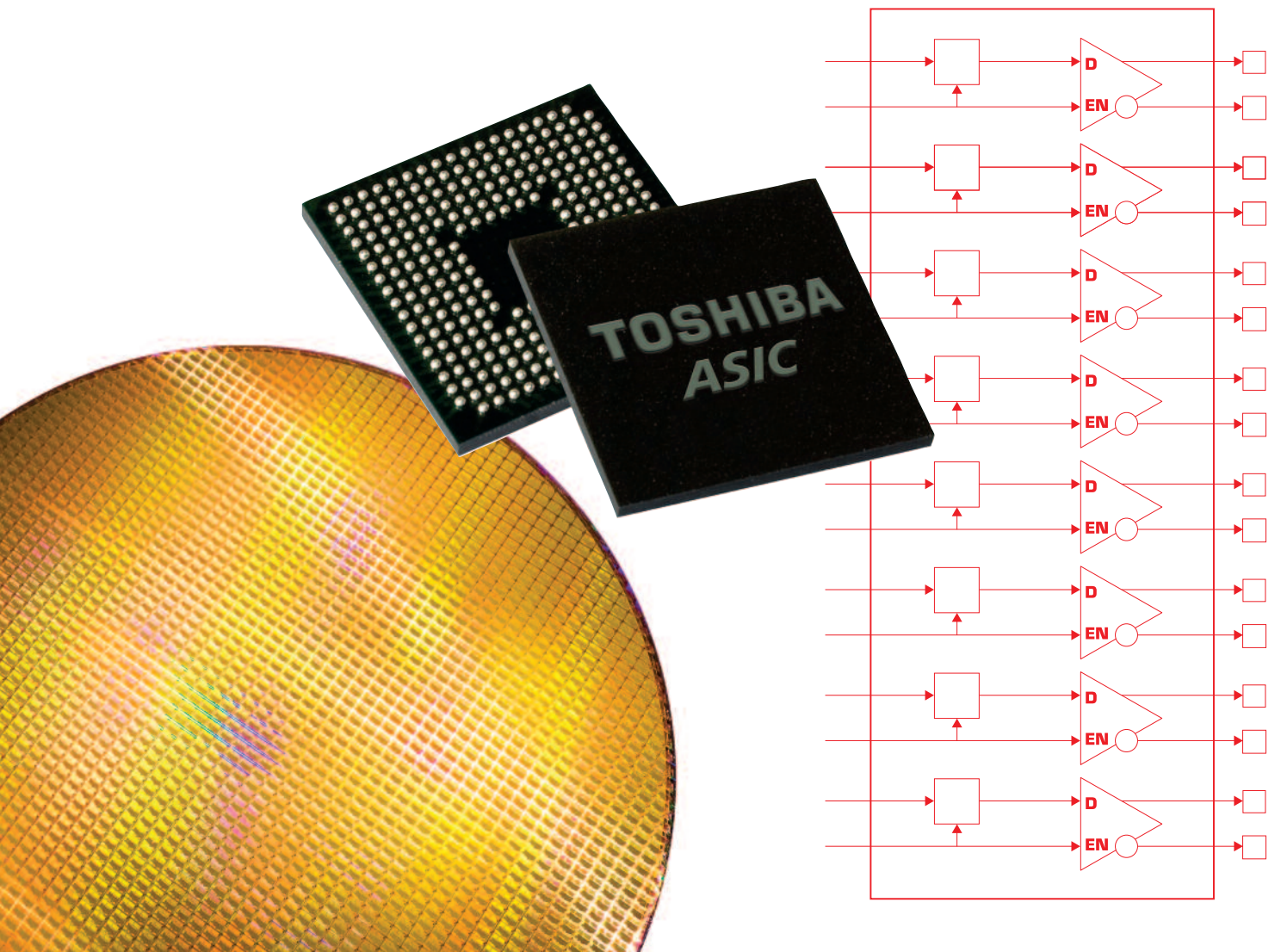
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> **ASIC / SOC SOLUTIONS
FOR FLAT PANEL DISPLAYS**

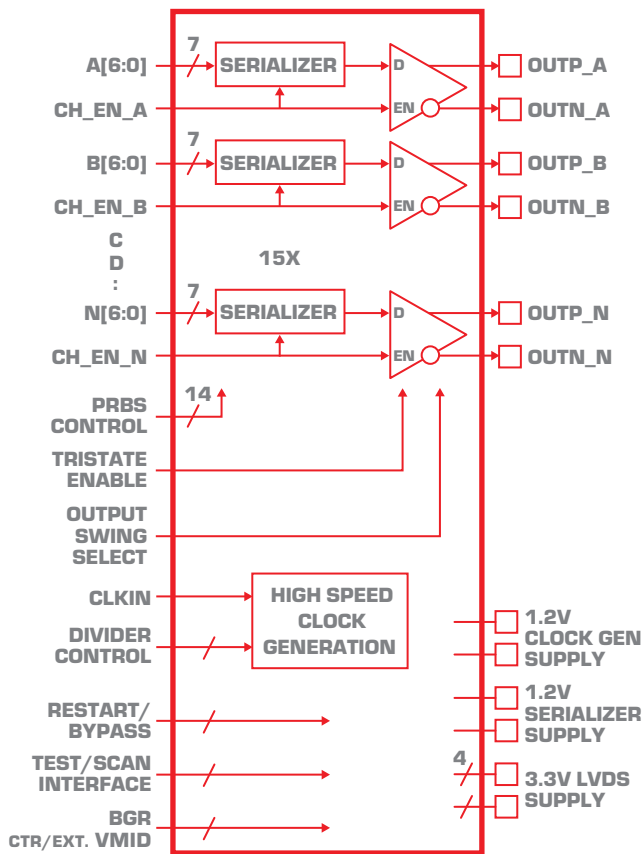
> **LVDS TRANSMITTER AND
RECEIVER MIXED-SIGNAL
IP CORE**



> FLAT PANEL DISPLAY LVDS TRANSMITTER DUAL LINK

Commonly employed in flat panel display (FPD) designs, LVDS is a signalling method for providing high-speed transmission of binary data over copper lines. The low-voltage differential swing is used to deliver higher transmission speeds and inherently higher bandwidths at lower power consumptions when compared to conventional single-ended transmission technologies.

Toshiba's LVDS transmitter is an IP block that provides an advanced, flexible and future-proofed solution for system designers looking to quickly and easily integrate dual link transmission from a host system-on-chip (SoC) ASIC to flat panel displays. Fully silicon-proven, this IP is compatible with FPDs delivering resolutions of up to UXGA.



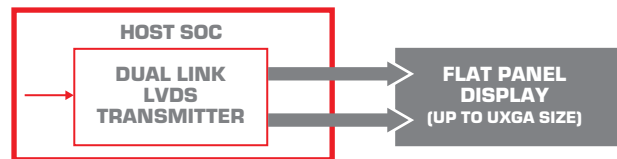
Offering seamless integration into Toshiba's advanced TC320 65nm (CMOS5) 1.2V low-power process, this IP block can convert up to 60 bits of RGB picture signal data and up to 12 bits of control signal data into 10 or 12 low-voltage differential swing (LVDS) streams.



In Dual Link mode at a transmit clock frequency of 85MHz, 72 bits of RGB and control data can be transmitted at an effective rate of 595Mbps per LVDS channel.

The dual link LVDS transmitter cell is supplied as a mixed-signal hard macro for direct integration into SoC products based on Toshiba's TC320 technology.

Operating at dot clock frequencies from 25MHz to 85MHz, the Toshiba Dual Link LVDS transmitter combines integrated high-speed clock generation and a selectable frequency range to minimise the need for external components. All links can be independently selected as clock line or data/control line.

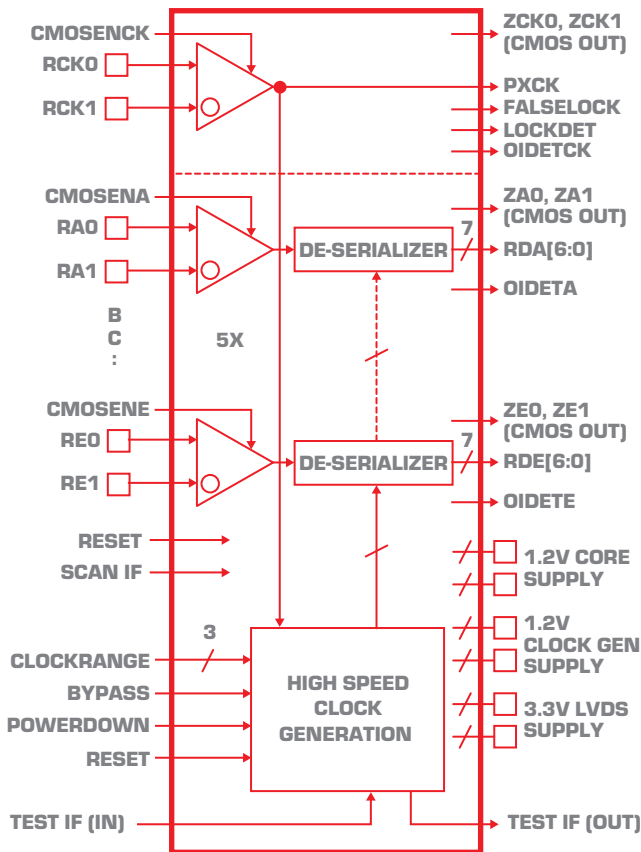


FEATURES AND BENEFITS

Dual LVDS transmitter link
Input clock range: 25~85MHz
Optional scalable channel setup (on customer request)
Parallel to serial data conversion included
Integrated high-speed clock generation (no requirement for external components)
Bandwidth up to 7.15Gbps with dual link
Power down mode (Individually selectable for each channel's serializer+LVDS buffer)
Frequency range selectable for optimum feedback divider / pre-divider / output divider ratio of high-speed clock generation block
Output swing selectable: Normal range (250~450mV) and reduced range (150~300mV)
Output tri-state switchable
Integrated test mode, scan mode for logic, direct access and bypass functions
Integrated test circuits for BIST (Built-In Self Test)
1.2V and 3.3V power supply
Typ. TX power per channel: 30mW
Power down mode: typ. TX power < 1mW
Integrated clock generation / Common block power: 20mW
Channel skew: Values of < 75ps can be achieved through appropriate package design
Differential skew: Values of < 20ps can be achieved through appropriate package design

➤ FLAT PANEL DISPLAY (FPD) LVDS RECEIVER LINK

Toshiba's LVDS receiver link is an IP block that provides an advanced, flexible, and future-proofed solution for system designers looking to quickly and easily integrate LVDS receivers into system-on-chip (SoC) display drivers for flat panel displays. Fully silicon-proven, this IP is compatible with FPDs delivering resolutions of up to SXGA+.

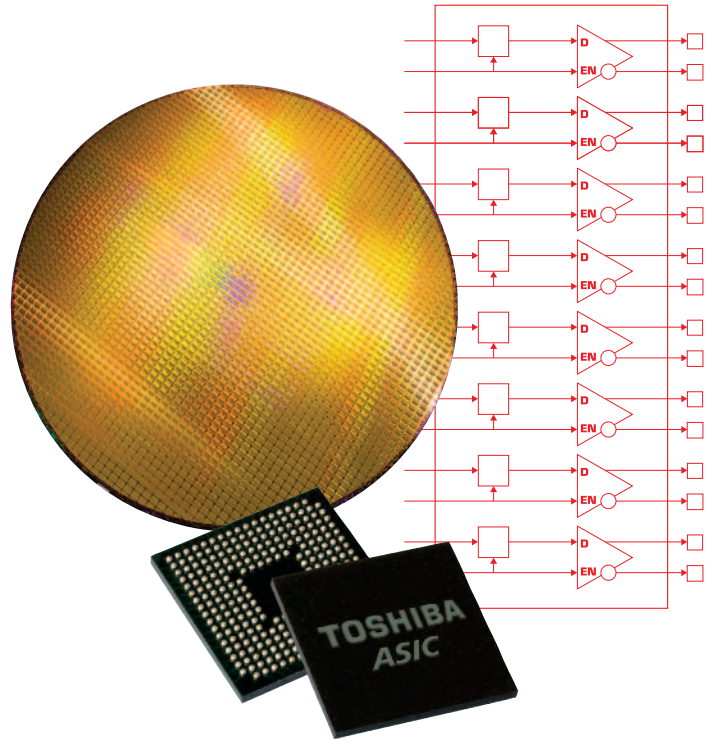


Offering seamless integration into Toshiba's advanced TC320 65nm (CMOS5) 1.2V low-power process, this IP block receives synchronous data along with the corresponding pixel clock information via an LVDS interface.

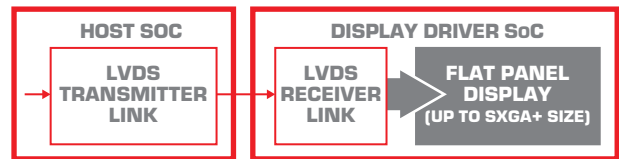
Incoming data is sampled by an internally generated high-speed clock and differential serial data is converted into a 7-bit parallel CMOS output for each channel by each pixel clock cycle.



This IP supports single link transmission between the host and the LVDS link at clock speeds of up to 150MHz. For frequencies below 20MHz, the cell offers LVDS feed-through signals to the SoC core. An on-chip high-speed clock generation block is used to multiply the received clock signal and synchronise it with the incoming data.



Operating at dot clock frequencies from 20MHz to 150MHz, the Toshiba LVDS receiver can handle data rates of 1.05Gbps per channel and offers a selectable frequency range for optimum high-speed clock generation set-up.



FEATURES AND BENEFITS

- LVDS receiver link
- 20MHz to 150MHz dot clock up to SXGA+ (1.05Gbps per channel)
- Optional scalable channel setup (on customer request)
- Open input detection for LVDS cells
- Serial to parallel data conversion included
- Integrated high-speed clock generation block: no requirement for external components
- Multi purpose I/O (LVDS or dual individual standard CMOS 3.3V inputs)
- Optional: LVDS on-chip termination
- Frequency range selectable for optimum setup of DLL
- Power down mode: typ. RX power < 1mW
- Typ. RX power: < 210mW (5 data channels incl. clock and DLL@85MHz)
- Test mode, scan mode for logic, boundary scan and bypass functions integrated
- Data/clock functional feed through mode
- 1.2V and 3.3V power supply

➤ TOSHIBA'S FPD IP WITH INTEGRATED LVDS TRANSCEIVERS

Toshiba's FPD-RX and FPD-TX IP solutions allow designers to quickly and easily create system-on-chip (SoC) ASICs that integrate LVDS transmitter and receiver functionality. Fully compatible with the Toshiba TC320 65nm low-power ASIC process, these advanced cells provide high levels of functionality and flexibility and are fully silicon-proven.

Each FPD IP block is supplied as a mixed-signal hard macro and GDSII, abstracts, models for major EDA tools and detailed application notes are all available. In standard cell implementations described above, Toshiba can also offer other configurations including solutions with different numbers of LVDS channels and other frequency ranges.

➤ SUPPORTING SOC IMPLEMENTATION

To speed and simplify the implementation of SoCs based on the company's advanced CMOS processes, Toshiba offers a variety of development handover models including:

ASIC MODEL

- RTL handover with synthesis, place-and-route, and verification by Toshiba or gate-level handover with synthesis by customer and layout implementation by Toshiba

SEAMLESS "HYBRID" MODELS

- Mixed-signal IP/block development by customer based on PDK, and chip-level integration by Toshiba (RTL handover or gate-level handover)

FULL COT (CUSTOMER OWN TOOLING) MODEL

- Physical data handover (GDSII) by customer.

In each handover model, engineers at Toshiba's local European Design and Engineering Center (ELDEC) are available to provide full technical support, advice and guidance relating to the integration-, QA- and testing of the FPD IP.

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GERMANY

TOSHIBA ELECTRONICS EUROPE GMBH CENTRAL EUROPEAN SALES

Hansaallee 181, 40549 Düsseldorf
Tel.: +49 (0211) 5296 0
Fax.: +49 (0211) 5296 400

FRANCE

TOSHIBA ELECTRONICS EUROPE GMBH, FRANCE BRANCH

Les Jardins du Golf, 6 rue de Rome,
F-93561 Rosny-Sous-Bois, Cédex, Paris
Tel.: +33 (1) 48 12 48 12
Fax.: +33 (1) 48 94 51 15

ITALY

TOSHIBA ELECTRONICS EUROPE GMBH, ITALY BRANCH

Centro Direzionale Colleoni, Palazzo Perseo
Ingresso 3, Via Paracelso 14, I-20041
Agrate Brianza, Milan
Tel.: +39 (039) 68701
Fax.: +39 (039) 6870205

UK

TOSHIBA ELECTRONICS EUROPE GMBH, UK BRANCH

Delta House, The Crescent,
Southwood Business Park,
Farnborough, Hampshire GU14 0NL
Tel: +44 (0870) 0602370
Fax: +44 (01252) 530250

SPAIN

TOSHIBA ELECTRONICS EUROPE GMBH, SPAIN BRANCH

Parque Empresarial, San Fernando, Edificio
Europa, 1ª Planta, E-28831 Madrid
Tel.: +34 (91) 660 6798
Fax.: +34 (91) 660 6799

SWEDEN

TOSHIBA ELECTRONICS EUROPE GMBH, SWEDEN BRANCH

Gustavslundsvägen 18, 5th Floor,
S-167 15 Bromma
Tel.: +46 (08) 704 0900
Fax.: +46 (08) 80 8459

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