

# Minimising SoC Risk - Evolving Business Models



By Armin Derpmanns, Toshiba Electronics

**It has become evident that when it comes to delivering next-generation designs, companies must re-evaluate their position in the overall value chain and think carefully about how that position will influence their choice of partner.**

**T**he move to new and emerging 90 and 65nm process geometries offers unprecedented potential for companies to deliver SoC-based designs offering better performance, higher levels of integration and more advanced functions than could have been imagined even just a few years ago. However, the potential risk and cost is also greater than ever before, so much so that the decision to create a new product using the latest process geometry can no longer be based on design issues alone. There are many other critical factors beyond the design arena that must now be taken into account, not least the company's position in the value chain in terms of delivering the total system solution.

For the companies that successfully address these issues, the rewards will, indeed, be great. However, with the cost of developing a 65nm chip running into tens of millions of dollars, and with the time from initial concept to volume production extending to three years or more, for those companies that get it wrong, the impact could be catastrophic.

The key questions that a company should be asking before embarking on the SoC journey are:

- How are we going to reach our market window?
- Does the organisation have the competence to cope with the total design work?
- How can manufacturing and yield issues be anticipated in the design phase?
- What is the core value we are adding within the overall value chain needed to bring the design to effective volume production?
- What element of the value chain must our partners provide?
- What criteria should we take into account when selecting the most appropriate partners for this venture?

Furthermore, one must consider the responses to these questions keeping in mind that the underlying business model for next-generation SoC developments is, by necessity, changing. In particular, it is becoming increasingly clear that the fully fragmented business model based on a number of different parties - independent design houses, IP companies, the EDA partners, foundries, assembly companies, test houses, etc. - is not the right model for delivering technically and commercially successful designs based on the newer geometries. Instead, what is needed is a faster and more effective feedback loop in which production expertise can be quickly fed into the design and development process.

## ⇒ The new landscape

One of the reasons that the business model is changing is that the new processes demand much higher levels of customisation, which, in turn, adds to the level of risk - threat that the necessary competence and expertise are not available; that costs will spiral; that the development deadlines will not be met; or that the custom solution does not lend itself to the final manufacturing process. And that risk increases with the number of different organisations needed to get the product from the

drawing board to the consumer. Probably the greatest challenge is creating a design that is optimised for the semiconductor-fabrication process, where the need for the fast and effective feedback loop comes in. Such a feedback loop is almost impossible to establish in the fragmented model, and lends itself much more readily to partners that have control over as much of the value chain as possible. Such partners are in the best position to deliver specific solutions that can minimise overall cost and time risks.

The new process geometries are re-writing the rules determining what the engineer can do; moreover, the need for the team involved in the design to have an in-depth understanding of the semiconductor technology is greater than before. In reality, only the companies who can fabricate the 90 and 65nm ICs have the depth of knowledge needed for such optimisation. By definition this precludes many fabless semiconductor vendors who will have to re-assess their approach in the light of where they are now placed within the new value-chain model. What we are saying, therefore, is that while a "plug-and-play" approach to ASSP and SoC design is desirable, it is not always possible. Today, the value that companies have to bring to the market must include system-level consultancy, software and hardware evaluation, and the capability to manage the requisite levels of integration. To support this emerging business, models will be based around a de-fragmentation and re-grouping of the market, with organisations wanting to work closely with one partner that has the vertical integration infrastructure needed to own, manage, add value to and optimise every element in the chain, from design to volume-manufacture process. As well as having control over wafer fabrication, these IDMs offer qualification and libraries, IP development, support and qualification, as well as full-scale silicon implementation services. This is the only way to achieve reliable turnaround and avoid costly re-spins.

## ⇒ Back to the basics

Choosing the right business partner for an SoC development has never been more critical, and, with the latest geometries, that choice must now come down to who is best positioned to bring the design to successful volume manufacture in the most cost-effective and timely manner possible. Before starting their SoC design and choosing the right partner, companies must fully understand their own value proposition. In particular, in a world where silicon optimisation and control are no longer likely to be the differentiator, they must look closely at how they focus on the creation and the marketing of their product, but also at all of the other "non-silicon" aspects needed to deliver a meaningful competitive advantage.