

Figure 2 91. Transmitted Data Hold Time at End of Transmit

b. 8-bit Receive Mode

Set the control register to receive mode and the SIOS to "1" for switching to receive mode. Data is received from the SI pin to the shift register in synchronous with the serial clock, starting from the least significant bit (LSB). When the 8-bit data is received, the data is transferred from the shift register to the SBIDBR. The INTSRI (buffer full) interrupt request is generated to request of reading the received data. The data is then read from the SBIDBR by the interrupt service program.

When the internal clock is used, the serial clock will stop and automatic-wait function will be initiated until the received data is read from the SBIDBR.

When the external clock is used, since shift operation is synchronized with the clock pulse provided externally, the received data should be read from the SBIDBR before next serial clock is input. If the received data is not read, further data to be received is canceled. The maximum transfer speed when the external clock is used is determined by the delay time between the time when an interrupt request is generated and the time when received data is read.

Receiving data is ended by clearing the SIOS to "0" by the buffer full interrupt service program or setting the SIOINH to "1". When the SIOS is cleared, received data is transferred to the SBIDBR in complete blocks. The received mode ends when the transfer is complete. In order to confirm if data is surely received by the program, set the SIOF (bit 3 in the SBIDBR) to be sensed. The SIOF is cleared to "0" when receiving is complete. After confirming that receiving has ended, the last data is read. When the SIOINH is set, receiving data stops. The SIOF turns "0" (the received data becomes invalid, therefore no need to read it).

Note: When the transfer mode is switched, the SBIDBR contents are lost. In case that the mode needs to be switched, receiving data is concluded by clearing the SIOS to "0", read the last data, and then switch the mode.

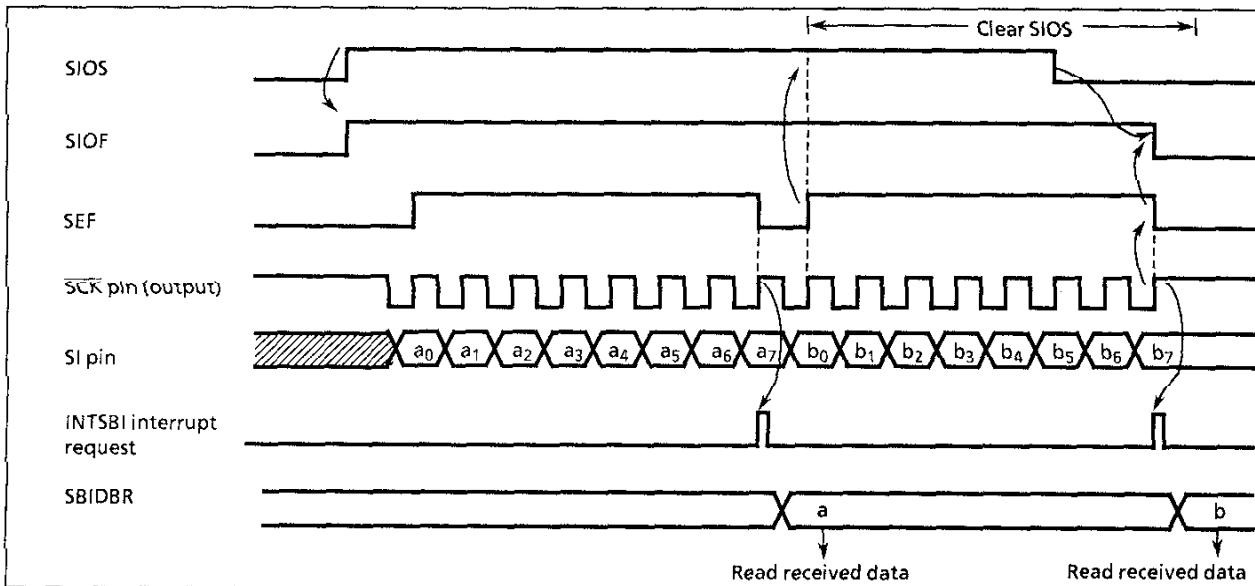


Figure 2-92. Receive Mode (Example: Internal clock)

c. 8-bit Transmit / Receive Mode

Set a control register to a transmit / receive mode and write data to the SBIDBR. After the data is written, set the SIOS to "1" to start transmitting / receiving. When transmitting, the data is output from the SO pin on the leading edges in synchronous with the serial clock, starting from the least significant bit (LSB). When receiving, the data is input to the SI pin on the trailing edges of the serial clock. 8-bit data is transferred from the shift register to the SBIDBR, and the INTSBI interrupt request occurs. The interrupt service program reads the received data from the data buffer register and writes data to be transmitted. The SBIDBR is used for both transmitting and receiving. Transmitted data should always be written after received data is read.

When the internal clock is used, automatic-wait function is initiated until received data is read and next data is written.

When the external clock is used, since the shift operation is synchronized with the external clock, received data is read and transmitted data is written before new shift operation is executed. The maximum transfer speed when the external clock is used is determined by the delay time between the time when an interrupt request is generated and the time when received data is read and transmitted data is written.

When the transmit is started, after the SIOF goes "1" output from the SO pin holds final bit of the last data until falling edge of the SCK.

Transmitting / receiving data is ended by clearing the SIOS to "0" by the INTSBI interrupt service program or setting the SIOINH to "1". When the SIOS is cleared, received data is transferred to the SBIDBR in complete blocks. The transmit / receive mode ends when the transfer is complete. In order to confirm if data is surely transmitted / received by the program, set the SIOF (bit3 in the SBISR) to be sensed. The SIOF becomes "0" after transmitting / receiving is complete. When the SIOINH is set, transmitting / receiving data stops. The SIOF turns "0".

Note: When the transfer mode is switched, the SBIDBR contents are lost. In case that the mode needs to be switched, conclude transmitting / receiving data by clearing the SIOS to "0", read the last data, and then switch the transfer mode.

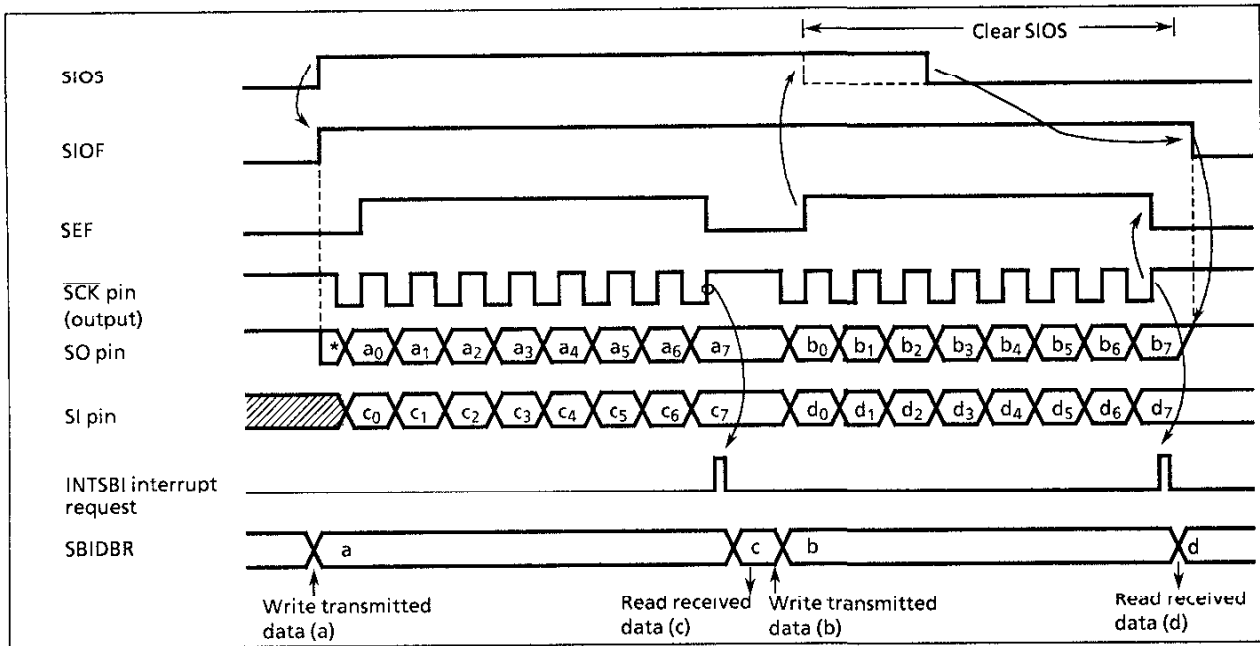


Figure 2-93. Transmit / Receive Mode (Example: Internal clock)

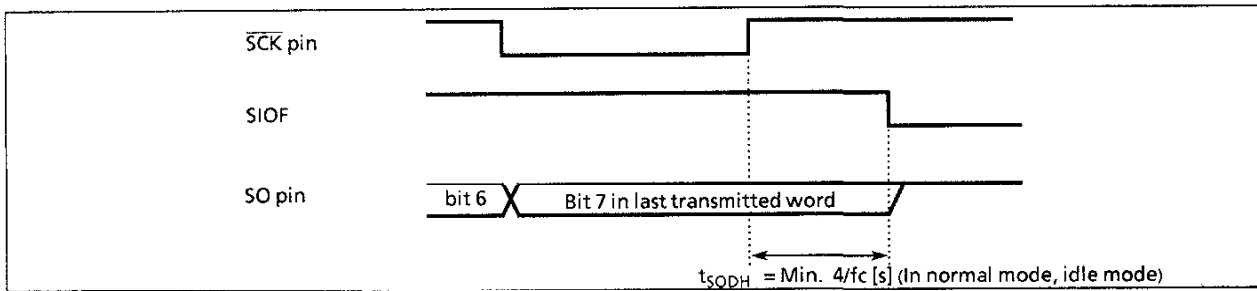


Figure 2-94. Transmitted Data Hold Time at End of Transmit / Receive

2.13 10-bit AD Converter (ADC)

2.13.1 Configuration

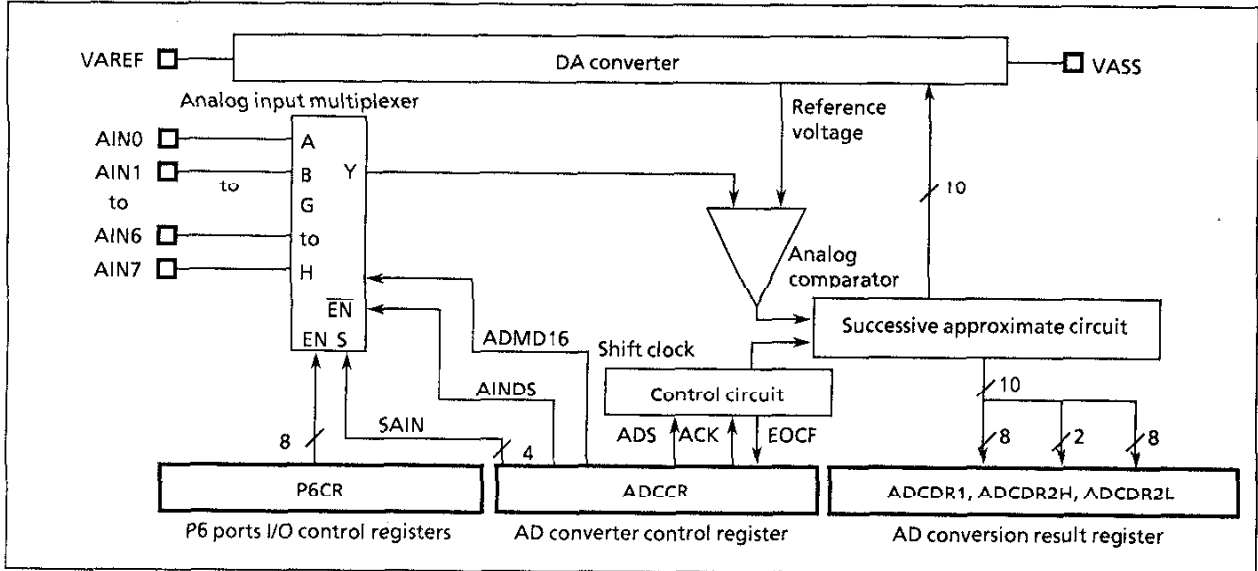


Figure 2-95. AD Converter (ADC)

2.13.2 Control

The AD converter is controlled using the AD converter control register (ADCCR), port P6 I/O control register (P6CR). Reading EOCF in ADCCR detects the AD converter operating status; reading AD conversion data register (ADCDR1) or (ADCDR2H), (ADCDR2L) detects AD conversion value.

AD converter control register

ADCCR (000E _H)	7	6	5	4	3	2	1	0	(Initial value: 0000 0000)
	EOCF/ ADMD16	ADS	ACK	AINDS	SAIN				
SAIN	Analog input channel select		0000: Selects AIN00. 0001: Selects AIN01. 0010: Selects AIN02. 0011: Selects AIN03. 0100: Selects AIN04. 0101: Selects AIN05. 0110: Selects AIN06. 0111: Selects AIN07.					R/W	
AINDS	Analog input control		0: Analog input enable 1: Analog input disable						
ACK	Conversion time select		0: 184/ <i>f_c</i> (11.5 μ s at 16 MHz) 1: 736/ <i>f_c</i> (46 μ s at 16 MHz)						
ADS	AD conversion start		0: - 1: AD conversion start					Read only	
EOCF	AD conversion end flag		0: Under conversion or before conversion 1: End of conversion						
ADMD16	Number of analog channels switch		0: Selects 8 channels. (AIN00 to 07) 1: reserved					Write only	

Note 1: The analog input channel must be selected when the AD conversion is stopped.
 Note 2: The ADS is automatically cleared to "0" after starting the AD conversion.
 Note 3: The EOCF is cleared to "0" by reading the AD conversion registers such as ADCDR1, ADCDR2H, or ADCDR2L.
 Note 4: The EOCF is read-only, so the written data is invalid.
 Note 5: ADMD16 is write-only; cannot be read. Write "0" to ADMD16.
 Note 6: *f_c*; High-frequency clock [Hz]

Figure 2-96. AD Converter Control Register

AD conversion data registers

ADCDR1 (000F _H)	7	6	5	4	3	2	1	0	Read only
	DATA9	DATA8	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	
ADCDR2H (0025 _H)	7	6	5	4	3	2	1	0	Read only
	1	1	1	1	1	1	DATA9	DATA8	
ADCDR2L (0024 _H)	7	6	5	4	3	2	1	0	Read only
	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	

Port P6 I/O control register

P6CR (000C _H)	7	6	5	4	3	2	1	0	(Initial value: 0000 0000)	
P6CR	I/O control for port P6 (specified for each bit)						0: 1:	As listed below		Write only
ADCCR		P6CR								
ADMD16	AINDS	0			1					
0	0	Input port except for the analog input selected by SAIN			Output port except for the analog input selected by SAIN					
1	0	Input port			Output port					
0	1	Input port			Output port					
1	1	Input port			Output port					

Figure 2-97. AD Conversion Register and Ports P6 I/O Control Register

2.13.3 AD Converter operation

Apply the analog reference voltage high side to the VAREF pin; apply the analog reference voltage low side to the VASS pin. AD conversion is performed by dividing, using a ladder resistor, the reference voltage between VAREF and VASS into voltages corresponding to bits and comparing the divided voltage with analog input voltage.

Note: $VAREF \leq VDD$ Please meet this condition by all means.

(1) Starting AD conversion Example with port P6 (AIN00 to AIN07)

Before AD conversion, select a pin among analog input channel pins (AIN7 to AIN0) using SAIN (bits 3 to 0 in ADCCR). Zero-clear AINDS (bit 4 in ADCCR) and sets a channel to be used for analog input to 1 using port P6 I/O control register (P6CR).

Note: The pin that is not used as an analog input can be used as regular input/output pins. During conversion, do not perform output instruction to maintain a precision for all of the pins.

Sets the AD conversion time using ACK (bit 5 in ADCCR).

The AD conversion is started by setting 1 in ADS (bit 6 in ADCCR).

When ACK = 0, a minimum of $184/f_c$ [s] (46 machine cycles) is required from AD conversion start to conversion result set in ADCDR1 or ADCDR2H/ADCDL2L. For example, when $f_c = 8$ MHz, the AD conversion time is 23 μ s. When AD conversion ends, EOCF (bit 7 in ADCCR) is set to 1 indicating conversion end.

Setting ADS to 1 during AD conversion initializes and starts conversion from the beginning again.

(2) Reading AD converted value

Read the conversion value stored in the AD conversion data register ADCDR1 or ADCDR2H/ADCDL2L after checking conversion end (EOCF = 1). Reading the conversion value automatically zero-clears EOCF. If EOCF is read during AD conversion, an undefined value is read.

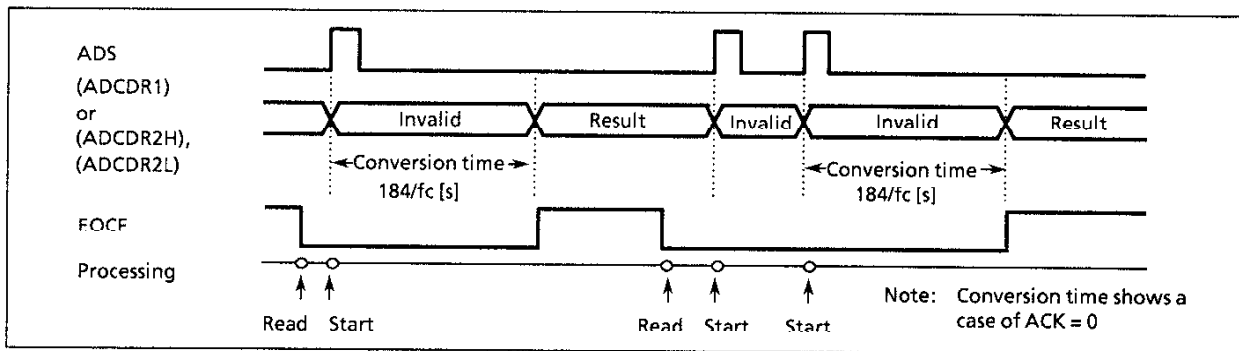


Figure 2-98. AD Conversion Timing Chart

(3) AD conversion in STOP mode

Entering STOP mode during AD conversion aborts AD conversion; the AD conversion value becomes undefined. Thus, after return from STOP mode, EOCF remains 0. Entering STOP mode after AD conversion end (EOCF = 1), the AD conversion value and EOCF status are retained.

Example: After the AIN04 pin is selected as an analog input channel, perform AD conversion. Check EOCF, read the conversion value, store upper 2 bits at address 009EH in RAM; lower 8 bits at address 009EH.

```
; AIN SELECT
LD      (ADCCR), 00100100B      ; Selects conversion time and AIN04.
; AD CONVERT START
LD      (ADCCR), 01100100B
SLOOP: TEST   (ADCCR). 7        ; EOCF = 1 ?
JRS     T, SLOOP
; RESULT DATA READ
LD      (9EH), (ADCDR2H)
LD      (9FH), (ADCDR2L)
```

(4) Notes for the current consumption on the stop mode when using an AD converter

Note 1: Current consumption value (I_{DD}) on stop mode on D. C. Characteristics chart is not including the value between $V_{AREF} - V_{ASS}$ (I_{REF}). TMP88CH47 do not have function to cut current between $V_{AREF} - V_{ASS}$ (I_{REF}). To cut I_{REF} on stop mode, maintain V_{AREF} on open condition by external circuit, or same electrical potential of V_{ASS} .

Note 2: Turning to stop mode during the process of AD conversion ($ADCCR\ EOCF = 0$) aborts the operation though it does not cut electricity on analog comparator sometimes. Before turning to stop mode, check AD conversion end flag is "1". Moreover check $EOCF$ after AD conversion is finished, and when $EOCF$ turns to "1", read AD conversion values ($ADCDR1, ADCR2H, ADCR2L$) and turn to stop mode. Or if it has been turned to stop mode without reading AD conversion value, read them after stop mode has released since the values are maintained. Refer to flowchart 2-99 (a).

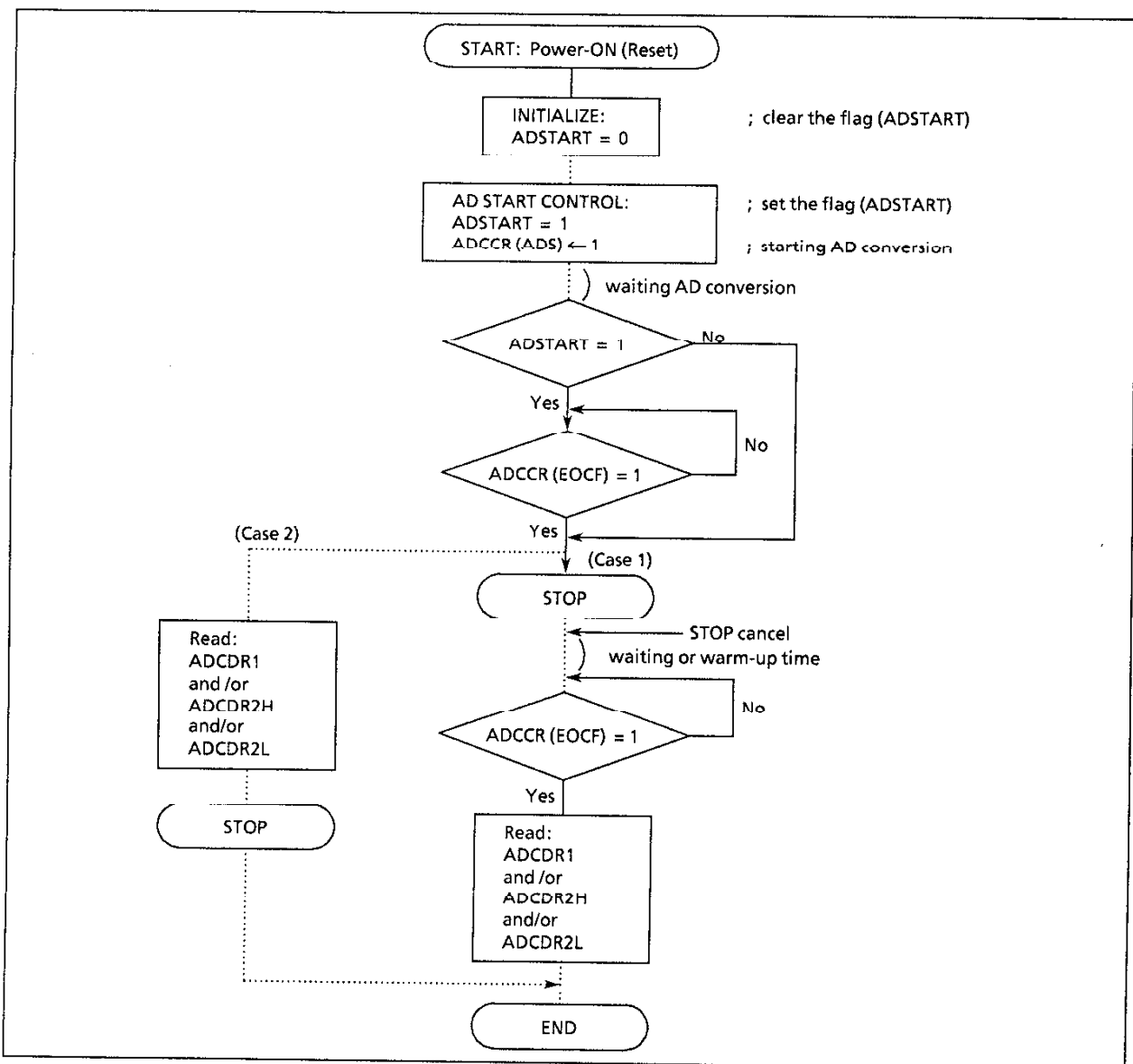


Figure 2-99 (a). Example Flow Chart for STOP Mode Control in the AD Converter System

(5) The relation between Analog Input Voltage and AD Conversion Result

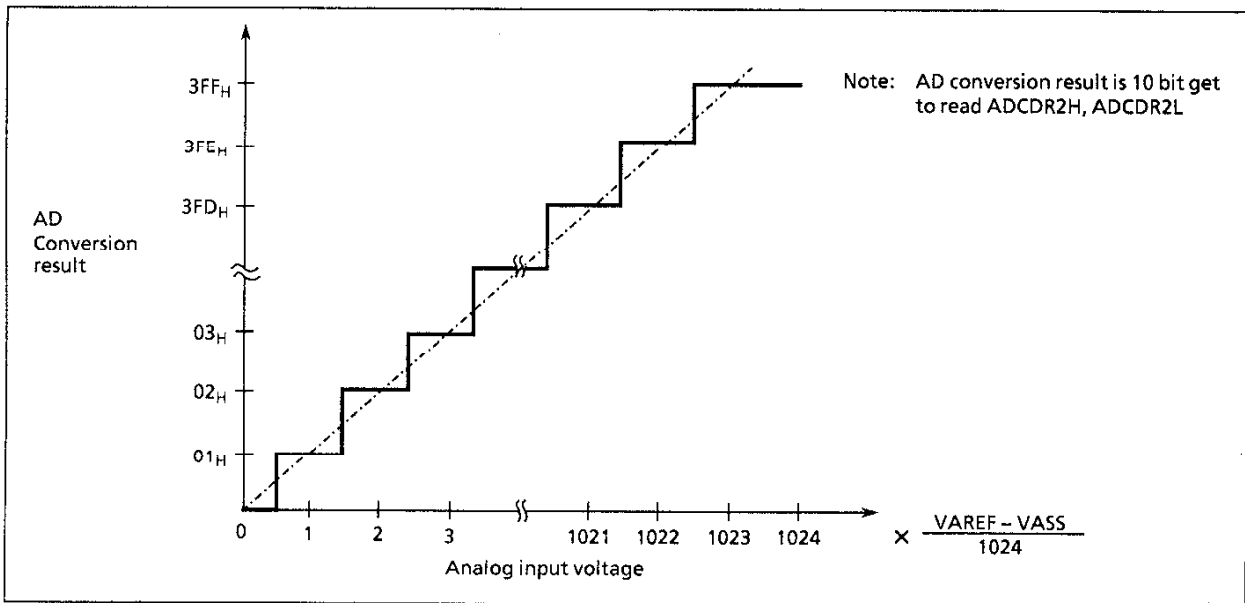


Figure2-99 (b). Analog Input Voltage vs AD Conversion Result (typ.)

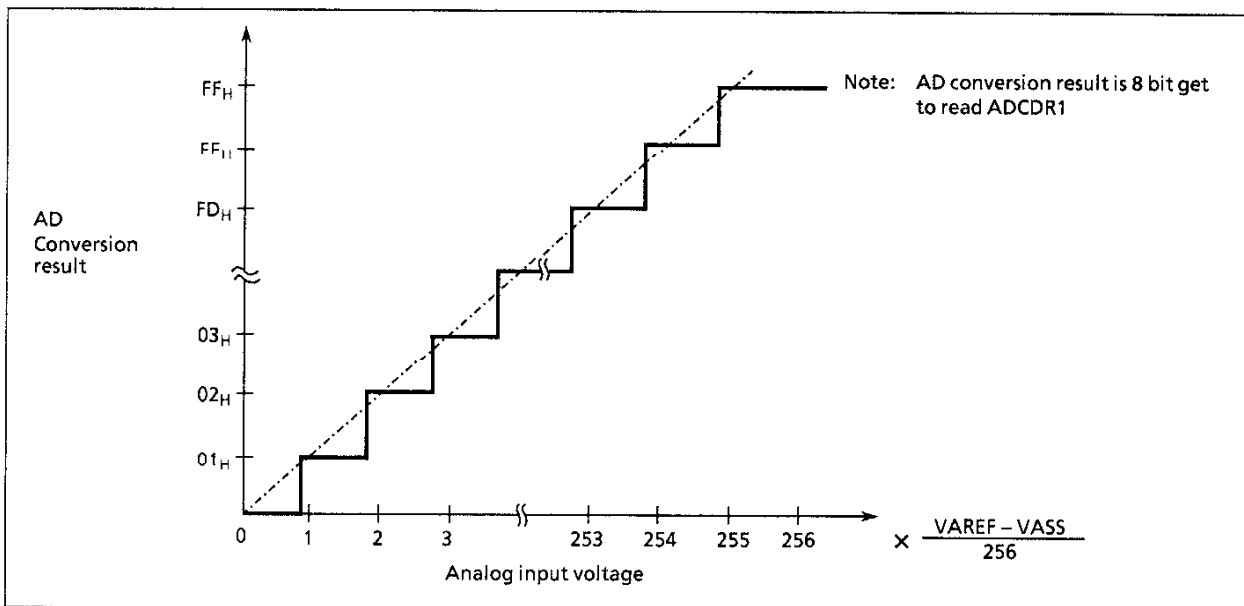


Figure2-99 (c). Analog Input Voltage vs AD Conversion Result (typ.)

Input / Output Circuit

(1) Control pins

The input / output circuits of the 88CH47 are shown below.

Control pin	I/O	Input / Output circuitry and Code	Remarks
XIN XOUT	Input Output		Resonator connecting pins (high-frequency) $R_f = 1.2\text{ M}\Omega$ (typ.) $R_o = 1.5\text{ k}\Omega$ (typ.)
$\overline{\text{RESET}}$	I/O		Sink open-drain output Hysteresis input Pull-up resistor $R_{IN} = 220\text{ k}\Omega$ (typ.) $R = 1\text{ k}\Omega$ (typ.)
$\overline{\text{STOP/INT5}}$	Input		Hysteresis input $R = 1\text{ k}\Omega$ (typ.)
TEST	Input		Pull-down resistor $R_{IN} = 70\text{ k}\Omega$ (typ.) $R = 1\text{ k}\Omega$ (typ.)

Note 1: The TMP88CH47 does not have a pull-down resistor for TEST pin. Must be fixed to "L" level.

Note 2: Insert a protection diode between V_{SS} or V_{DD} as close to the package as possible

(2) Input / Output ports

The input/output circuitries of the 88CH47 input/output ports are shown below.

Port	I/O	Input/Output circuitry and Code	Remarks
P0 P6	I/O	<p>initial "Hi-Z"</p>	<p>Tri-state I/O</p> <p>R = 1 kΩ (typ.)</p>
P1	I/O	<p>initial "Hi-Z"</p>	<p>Tri-state I/O</p> <p>Hysteresis input</p> <p>R = 1 kΩ (typ.)</p>
P4 P5	I/O	<p>initial "Hi-Z"</p>	<p>Sink open drain output</p> <p>R = 1 kΩ (typ.)</p>

Note: Insert a protection diode between V_{SS} or V_{DN} as close to the package as possible.

Electrical Characteristics

Absolute Maximum Ratings

 $(V_{SS} = 0\text{ V})$

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	V_{DD}		- 0.3 to 6.5	V
Input Voltage	V_{IN}		- 0.3 to $V_{DD} + 0.3$	V
Output Voltage	V_{OUT1}	Port P21, P22, $\overline{\text{RESET}}$, Tri-state port	- 0.3 to $V_{DD} + 0.3$	V
	V_{OUT2}	Port P20, Sink open drain port	- 0.3 to 5.5	V
Output Current	I_{OUT1}	Ports P1, P2, P4, P5, P6	3.2	mA
	I_{OUT2}	Port P0	20	
Output Current	ΣI_{OUT1}	Ports P1, P2, P4, P5, P6	120	mA
	ΣI_{OUT2}	Port P0	60	
Power Dissipation [$T_{opr} = 70^\circ\text{C}$]	PD	TMP88CH47	600	mW
Soldering Temperature (time)	T_{sld}		260 (10 s)	$^\circ\text{C}$
Storage Temperature	T_{stg}		- 55 to 125	$^\circ\text{C}$
Operating Temperature	T_{opr}		- 40 to 85	$^\circ\text{C}$

Note. The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions

 $(V_{SS} = 0\text{ V}, T_{opr} = -40\text{ to }85^\circ\text{C})$

Parameter	Symbol	Pins	Conditions	Min	Max	Unit	
Supply Voltage	V_{DD}		$f_c =$	4.5	5.5	V	
			16 MHz				NORMAL mode
							IDLE mode
		STOP mode					
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geq 4.5\text{ V}$	$V_{DD} \times 0.70$	V_{DD}	V	
	V_{IH2}	Hysteresis input		$V_{DD} \times 0.75$			
	V_{IH3}			$V_{DD} \times 0.90$			
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geq 4.5\text{ V}$	0	$V_{DD} \times 0.30$	V	
	V_{IL2}	Hysteresis input			$V_{DD} \times 0.25$		
	V_{IL3}				$V_{DD} \times 0.10$		
Clock Frequency	f_c	XIN, XOUT	$V_{DD} = 4.5\text{ to }5.5\text{ V}$	8.0	16.0	MHz	

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Clock frequency f_c : The condition of supply voltage range is the value in NORMAL and IDLE modes.

D.C. Characteristics

(V_{SS} = 0 V, Topr = -40 to 85°C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Hysteresis Voltage	V _{HS}	Hysteresis inputs		-	0.9	-	V
Input Current	I _{IN1}	TEST	V _{DD} = 5.5 V V _{IN} = 5.5 V/0 V	-	-	± 2	μA
	I _{IN2}	Sink open drain, Tri-state ports					
	I _{IN3}	RESET, STOP					
Input Resistor (*)	R _{IN}	TEST with pull-down		20	70	170	kΩ
	R _{IN}	RESET		90	220	510	
Output Leakage Current	I _{OL}	Sink open drain, Tri-state ports	V _{DD} = 5.5 V, V _{OUT} = 5.5 V/0 V	-	-	± 2	μA
Output High Voltage	V _{OH}	Tri-state ports	V _{DD} = 4.5 V, I _{OH} = -0.7 mA	4.1	-	-	V
Output Low Current	I _{OL1}	Except XOUT, Ports P0	V _{DD} = 4.5 V, V _{OL} = 0.4 V	-	1.6	-	mA
	I _{OL2}	Port P0	V _{DD} = 4.5 V, V _{OL} = 1.0 V	-	10	-	
Supply Current in NORMAL Mode			V _{DD} = 5.5 V V _{IN} = 5.3 V/0.2 V f _c = 16.0 MHz	-	20	32	mA
Supply Current in IDLE Mode				-	10	16	
Supply Current in STOP Mode				V _{DD} = 5.5 V V _{IN} = 5.3 V/0.2 V	-	0.5	20

Note 1: Typical values show those at Topr = 25°C, V_{DD} = 5 V.

Note 2: Input Current I_{IN1}, I_{IN3}: The current through resistor is not included, when the input resistor (pull-up or pull-down) is contained.

Note 3: I_{DD} except I_{REF}.

AD Conversion Characteristics

(Topr = -40 to 85°C)

Parameter	Symbol	Conditions	Min	Typ.	Max			Unit
					ADCDR1	ADCDR2		
						ACK = 0	ACK = 1	
Analog Reference Voltage	V _{AREF}	V _{AREF} - V _{ASS} ≥ 3.5 V	V _{DD} - 1.0	-	V _{DD}			V
	V _{ASS}		V _{SS}	-	1.0			
Analog Input Voltage	V _{AIN}		V _{ASS}	-	V _{AREF}			V
Analog Supply Current	I _{REF}	V _{AREF} = 5.5 V, V _{ASS} = 0.0 V	-	0.5	1.0			mA
Non-Linearity Error		V _{DD} = 5.0 V, V _{SS} = 0.0 V V _{AREF} = 5.000 V V _{ASS} = 0.000 V			± 1	± 3	± 2	LSB
Zero Point Error					± 1	± 3	± 2	
Full Scale Error					± 1	± 3	± 2	
Total Error						± 2	± 6	

Note 1: ADCDR1: 8-bit AD conversion result (1LSB = ΔV_{AREF}/256)

ADCDR2: 10-bit AD conversion result (1LSB = ΔV_{AREF}/1024)

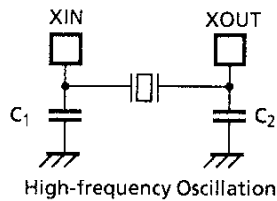
Note 2: Total error includes all errors except quantization error.

A.C. Characteristics (V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = -40 to 85°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	NORMAL mode	0.25	-	0.5	μs
		IDLE mode				
"H" Level Clock Pulse Width	t _{WCH}	For external clock operation (XIN input)	31.25	-	62.5	ns
"L" Level Clock Pulse Width	t _{WCL}					

Recommended Oscillating Conditions (V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = -40 to 85°C)

Parameter	Oscillator	Oscillation Frequency	Recommended Oscillator	Recommended Constant	
				C ₁	C ₂
High-frequency Oscillation	Ceramic Resonator	16 MHz	MURATA CSA16.00 MXZ	5pF	5pF
			MURATA CST16.00 MXW	built-in 5pF	built-in 5pF



Note: An electrical shield by metal shield on the surface of IC package should be recommendable in order to prevent the device from the high electric fieldstress applied from CRT (Cathode Ray Tube) for continuous reliable operation.