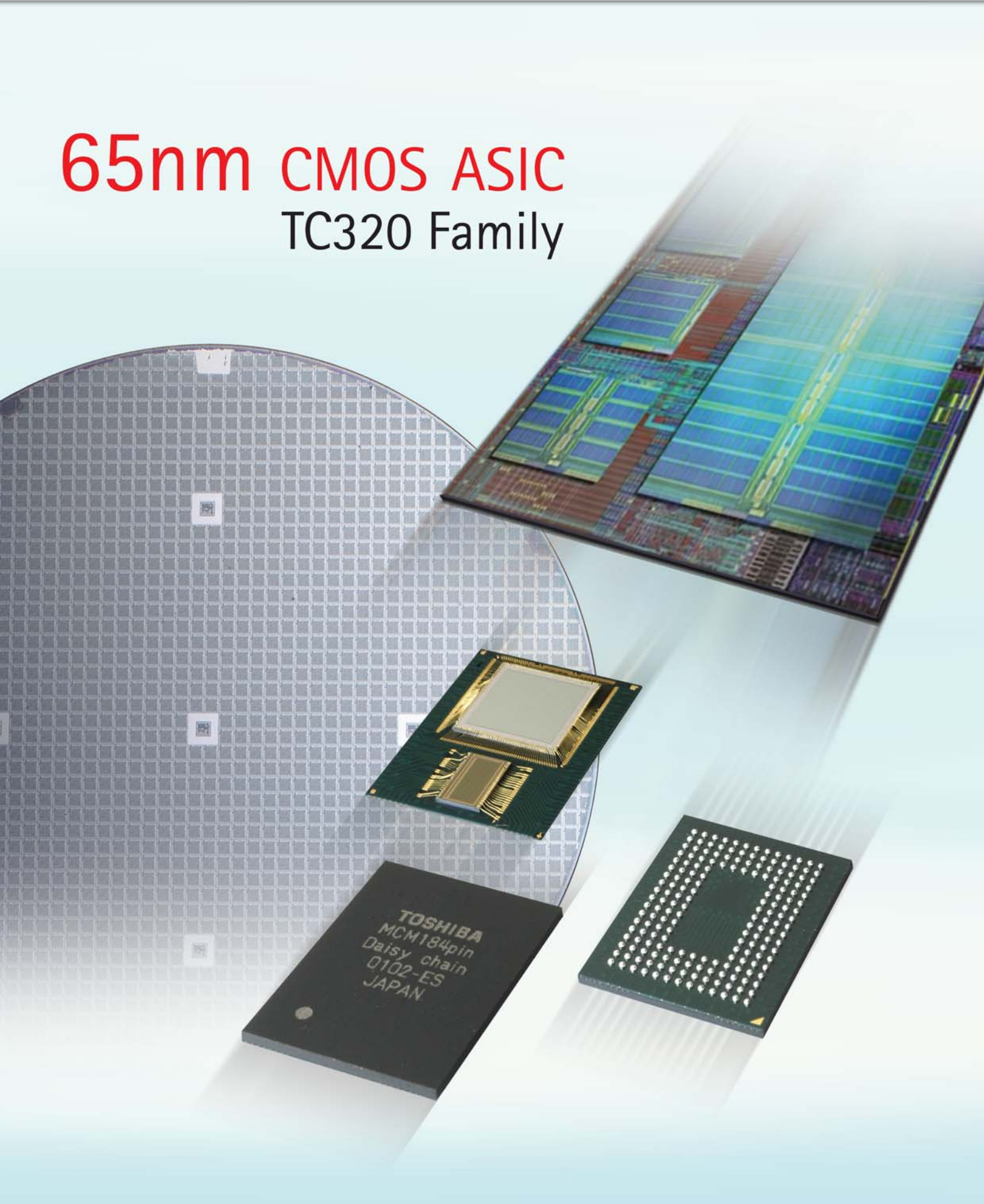


**TOSHIBA**  
Leading Innovation >>>

# 65nm CMOS ASIC

## TC320 Family



## Ultra-High Density SoC and SiP Solutions for Ultra-Low Power Applications

### 65nm (TC320) Family

Next generation consumer and mass market applications such as mobile phones and portable multimedia players demand highly integrated, single package system-on-chip (SoC) technologies with small footprint in order to achieve further miniaturization and to ensure ultra-low power consumption.

High-quality multimedia streaming and gaming applications are boosting integration levels, memory size and speed requirements to an ever higher level. At the same time, there is a need to widen the interface to components outside the system-in-package (SiP) by using high-speed serial links and double-data-rate parallel interfaces.

Thanks to Toshiba's advanced CMOS process, the ultra-high-density and the outstanding low power consumption of Toshiba's 65nm (TC320) family is ideally suited to satisfy these demanding requirements. The combination of low power and high density allows the integration of high-quality video and audio encoding without straining the extremely tight power budget of feature-rich mobile products, resulting in extended battery life.

The new 65nm process technology not only offers unprecedented embedded DRAM and tightly stacked semi-embedded DRAM capabilities, but also permits easy mixing of analog and application-specific IP cores on the same chip.

In addition to a multi-threshold process capability that allows mixing of logic cells operating at different threshold voltages, the optional 1.0V core voltage - along with other highly advanced power saving techniques such as conditional clocked low power Flip-Flops - allows for drastic cuts to both dynamic power consumption and leakage current.

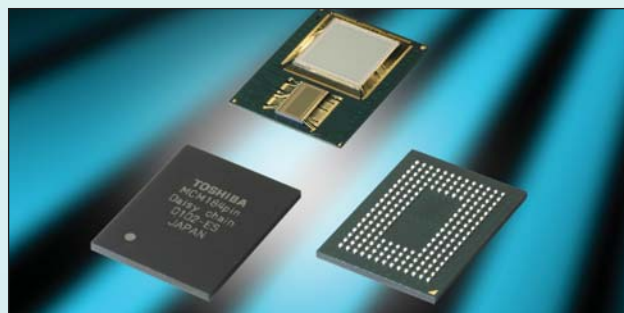
Low power ASIC implementation is further supported through leading edge low power design methodologies and technologies such as dynamic frequency and voltage scaling, placement aware clock gating and placement aware clock tree synthesis, as well as the ability to accurately analyze the power consumption of the device.

The TC320 family capitalizes on copper technology, low-k dielectric and the industry's most aggressive 65nm (50nm drawn gate) CMOS process. The process supports up to eight levels of copper metal plus one level of aluminium interconnect.

With the 65nm (TC320) family, Toshiba offers a robust, state-of-the-art design environment geared to shorten the development time for complex SiP designs incorporating high-speed interfaces.

This environment features an unparalleled concurrent Chip-Package-System development methodology that takes account of the package and silicon characteristics during the planning and implementation phase of the product.

Toshiba's 65nm (TC320) family offers an ideal solution for multimedia and low power portable applications, mobile phones and any other application where both high system integration and low power consumption are important criteria.



### Features and Benefits

#### Ultra-Low Power and Ultra-High Density

The 65nm (TC320) family is fabricated using the new CMOS5 process, which is a product of Toshiba's own process development. This leads to the forthcoming improvements over the 90nm (TC300) Family:

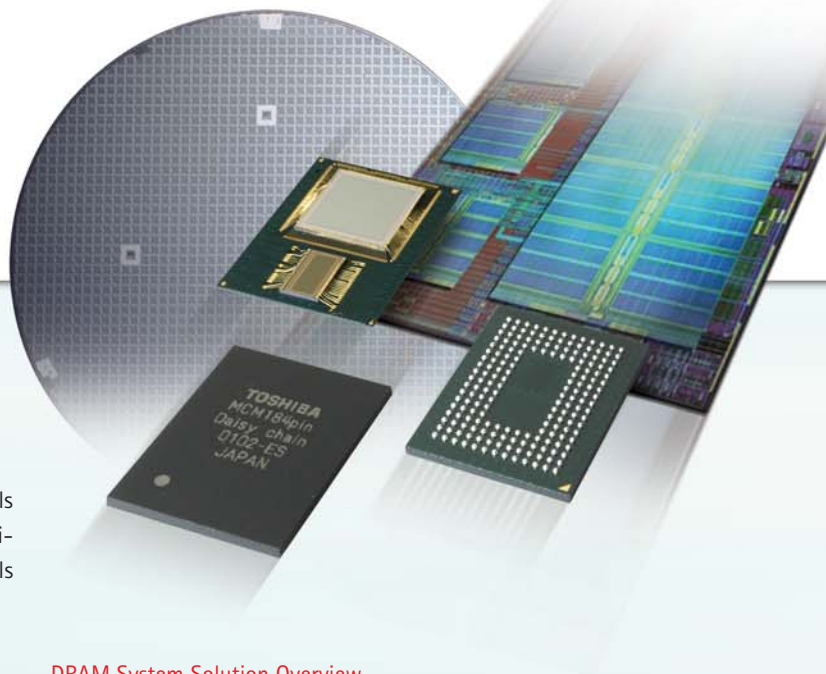
- x2 improvement in logic density
- 30% power saving per gate
- 20% reduction in gate delay

#### General Product Specification

Design Rule	65nm (50nm drawn gate), CMOS process, 8-layer Cu + 1-layer Al
Power Supply	Core=1.2V (1.0V option), analog=2.5V, I/O: 2.5V/3.3V (1.8V option)
Gate Delay (F/O=1, CQIVX4 Gate)	Three types of transistors are available with different threshold voltages: 10.2ps (Low-Power Library) 7.8ps (High-Speed Library) 7.2ps (Very-High-Speed Library)
Gate Density	800kgates/mm <sup>2</sup> or more
Power Dissipation	5.68nW/MHz/gate (F/O=0, CQIVX4)

#### Copper Interconnect

Up to eight levels of copper plus one level of aluminium wiring combined with low-k dielectric.



## Cell Library

### Primitive Cells

The 65nm (TC320) family offers synthesis-friendly primitive cells for both high-performance and low-power chip designs. The multi-threshold process provides the ability to mix and match the cells of both high-speed and low-power libraries.

### I/O Cells

The 65nm (TC320) family offers I/O cells in two shapes: narrow width I/O cells for high-pin-count designs and standard width I/O cells for core-limited designs.

### SRAMs

Compatible performance - and density-optimized single port and multiport SRAMs with flexible width and depth.

### IP Cores

Toshiba supports an ever-growing selection of mixed-signal and digital IP cores. These include VSI-compliant proprietary cores that have been developed in-house as well as IP cores from reliable partners.

ADC	Mobile TV, Communication, Video AFE, General Purpose
ARM	ARM7TDMI, ARM926, ARM946, ARM1136, ARM1176, Cortex™-M3
ATA	SATA (Gen1, Gen2*), PATA 66/100
Cryptography	DES, Triple DES, AES, MD5, SHA-1, SHA-256, Random Number Generator
DAC	Communication, Video DAC, General Purpose
Ethernet	10/100/1G Ethernet MAC
Fabric IP	VIC, UART, GPIO, I <sup>2</sup> C, SPI, Timer, DMA
HDMI	HDMI (Rev1.3) RX/TX, Source, Sink
Memory	DDR2, DDR3*, XIO*, SD card, SmartMedia™, MemoryStick PRO™
MIPI	D-PHY
MIPS	TX System RISC cores (Hardmacro)
PCI	PCI Express (Gen1/Gen2*), PCI 33/66
PLL	300M-1G Generic, $\Sigma\Delta$ Fractional PLL
USB	USB1.1, USB2.0 (1/2 port), OTG, Host, Device

\*Planned

ARM is a registered trademark of ARM Limited in Europe and the U.S.

### DRAM System Solution Overview

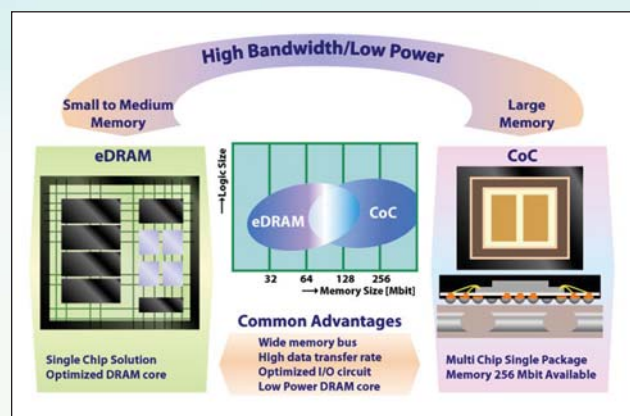
Depending on the DRAM size requirements, Toshiba offers embedded DRAM cores for small to medium memory sizes and a tightly stacked semi-embedded DRAM technology utilizing revolutionary Chip-on-Chip (CoC) technology that suits medium to extremely large DRAM sizes.

### Embedded DRAM Core Overview

The embedded DRAM cores based on Toshiba's leading trench capacitor technology provide many features, such as high memory bandwidth with a bus width selectable from 64, 128 and 256 bits, low power dissipation due to lower capacitance connections and low switching noise on the data bus between memory and logic. Easy integration is assured thanks to interface compliancy with the synchronous DRAM standard.

### Tightly-Stacked Semi-Embedded DRAM

High-quality multimedia applications for portable devices require high bandwidth access to a large DRAM memory without compromising on either power consumption or system footprint on the printed-circuit-board (PCB). Toshiba provides the ideal solution by directly connecting the DRAM silicon die face down via tiny micro bumps on the surface of the logic die and assembling the multi-chip solution into a standard package.



# TOSHIBA

## Leading Innovation >>>

## Design Methodology and Local Engineering Expertise Speed SoC and SiP Designs

Production-proven tools and methodology ensure predictable results and reduce design time and iterations for SoC and SiP ASICs

### Hierarchical Design

Toshiba provides local support for SoC and SiP designs via its European LSI Design & Engineering Centre (ELDEC). Hierarchical design approaches combined with a timing-driven design flow allows the ELDEC design team to create sub-blocks in parallel and resolve timing problems at the block level.

### Predictable Timing Closure

The advanced synthesis technique utilizes physical information to generate accurate wire models during RTL synthesis. This ensures a close correlation between pre-layout and post-layout delays. Accurate delay information is leveraged throughout the design flow, including design optimization (gate sizing), timing-driven routing and repeater insertion. As a result, timing closure can be achieved quickly.

### 3D Capacitance Extraction

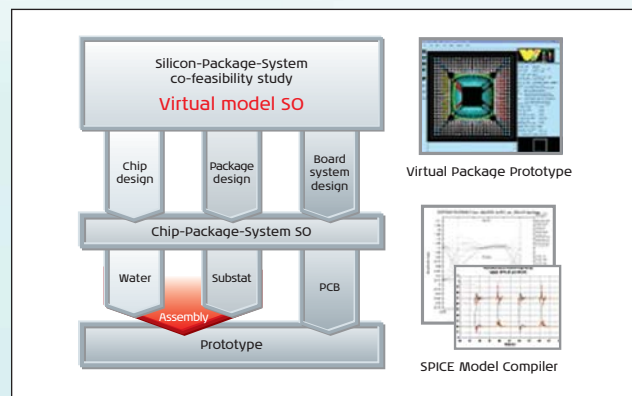
In today's deep-submicron ASICs, delays caused by interconnect are becoming increasingly dominant over gate delays. To accurately calculate deep-submicron delays, new techniques must be used. Toshiba employs 3D capacitance extraction to improve the accuracy of timing estimates for multi-layer metal processes.

### Signal Integrity Analysis and Repair

To ensure signal integrity, Toshiba optimizes power grid routing, based on IR drop estimation, early in the design cycle. Additionally, electromigration, antenna effects, hot-carrier injection (HCI) and negative bias temperature instability (NBTI) are all considered. The 65nm (TC320) design flow also embraces crosstalk analysis and elimination.

### Chip-Package-System (CPS)

Traditionally SoC and package design has been done separately, which can lead to unnecessary iterations and delays and very often result in a suboptimal silicon/package solution. By considering package, silicon and PCB characteristics at a very early stage of the implementation (during the feasibility study and planning phase), the quality of the overall product can be improved dramatically while enjoying a reduced development time.



## Packaging

Toshiba offers a complete range of packaging options, satisfying the requirements of advanced SiPs. For designs requiring high pin counts (600 to over 2000), Toshiba's flip-chip BGA packaging (PBGA[FC]) offers the highest I/O density and electrical performance available today. PBGAs with 109 to 265 pins have a package body size no larger than 15 x 15mm and are optimal for applications requiring minimal form factor. PBGAs with 256 to 868 pins are cost-effective solutions for mid-range I/O pin count requirements. In addition, Toshiba offers multi-layer PBGA[4L] packaging with excellent electrical performance for the 256 to 868 pin range. For price-sensitive applications with low pin-count, the extremely thin WCSP (Wafer Level Chip Scale Package) is the optimal solution. Toshiba provides the electrical models for its packages to help engineers select the optimal solution for every design specification.

GERMANY  
TOSHIBA ELECTRONICS EUROPE GMBH  
CENTRAL EUROPEAN SALES  
Düsseldorf  
Hansaallee 181  
40549 Düsseldorf  
Tel.: +49-211-5 29 60  
Fax.: +49-211-5 29 64 00

UK  
TOSHIBA ELECTRONICS (UK) LTD  
Farnborough  
Delta House, The Crescent  
Southwood Business Park  
Farnborough  
GU14 0NL  
Tel: +44-(0)1870-0602370  
Fax: +44-(0)1252-530250

FRANCE  
TOSHIBA ELECTRONICS FRANCE S.A.R.L.  
Paris  
Les Jardins du Golf  
6 rue de Rome  
93561 Rosny-Sous-Bois, Cédex  
Tel.: +33-1-48 12 48 12  
Fax.: +33-1-48 94 51 15

SPAIN  
TOSHIBA ELECTRONICS ESPAÑA S.A.  
Madrid  
Parque Empresarial  
San Fernando  
28831 Madrid  
Tel.: +34-1-6 60 67 98  
Fax.: +34-1-6 60 67 99

SWEDEN  
TOSHIBA ELECTRONICS SCANDINAVIA AB  
Bromma  
Gustavslundsvägen 18  
S-161 15 Bromma  
Tel.: +46-8-7 04 09 00  
Fax.: +46-8-80 84 59

ITALY  
TOSHIBA ELECTRONICS ITALIANA S.R.L.  
Milan  
Centro Direzionale Colleone  
Palazzo Perseo Ingresso 3  
20041 Agrate Brianza  
Tel.: +39-39-6 87 01  
Fax.: +39-39-6 87 02 05

[www.toshiba-components.com/ASIC](http://www.toshiba-components.com/ASIC)

TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc.

The Toshiba products listed on this document are intended for use in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). These Toshiba products are neither intended nor warranted for use in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury ("Unintended Usage"). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc. Unintended Usage of Toshiba products listed in this document shall

be made at the customer's own risk. The products described in this document may include products subject to the foreign exchange and foreign trade laws.

The information contained in this document is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA for any infringements of patents or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of TOSHIBA or others.

Copyright and published by Toshiba Electronics Europe GmbH; Hansaallee 181 - 40549 Düsseldorf  
Handelsregister Düsseldorf HRB 22487; Geschäftsführer: Ryoichi Shikama; Amtsgericht Düsseldorf

Products or company names mentioned herein are Trademarks of their respective owners.  
The information contained herein is subject to change without notice.