

TOSHIBA

PRODUCT GUIDE

SoC (System on a Chip) EDA



Toshiba's SoC EDA Tools Supporting its Cutting-Edge Silicon Technologies

High-performance systems-on-a-chip (SoCs) using over 10 million gates have now become a reality. ASIC/SoC designers now face the tremendous challenge of producing high-quality complex designs in a short amount of time. To meet a new set of challenges unique to SoC designs, new tools and methodologies are required. While design exploration must start at higher levels of abstraction to improve productivity, shrinking circuit geometries require that difficult physical issues be addressed from early in the design cycle.

For example, layout-based synthesis (physical synthesis) is becoming increasingly popular as a means of enabling rapid timing closure. At the same time, to prevent quality problems from worsening, we've worked on and improved the tools to resolve signal integrity issues such as voltage drop and crosstalk.

Furthermore, we embrace industry-leading EDA tools aggressively. Toshiba offers design environments built on and integrated into these tools.

All of them are in keeping with our overriding commitment to providing you with unsurpassed ASIC/SoC solutions.

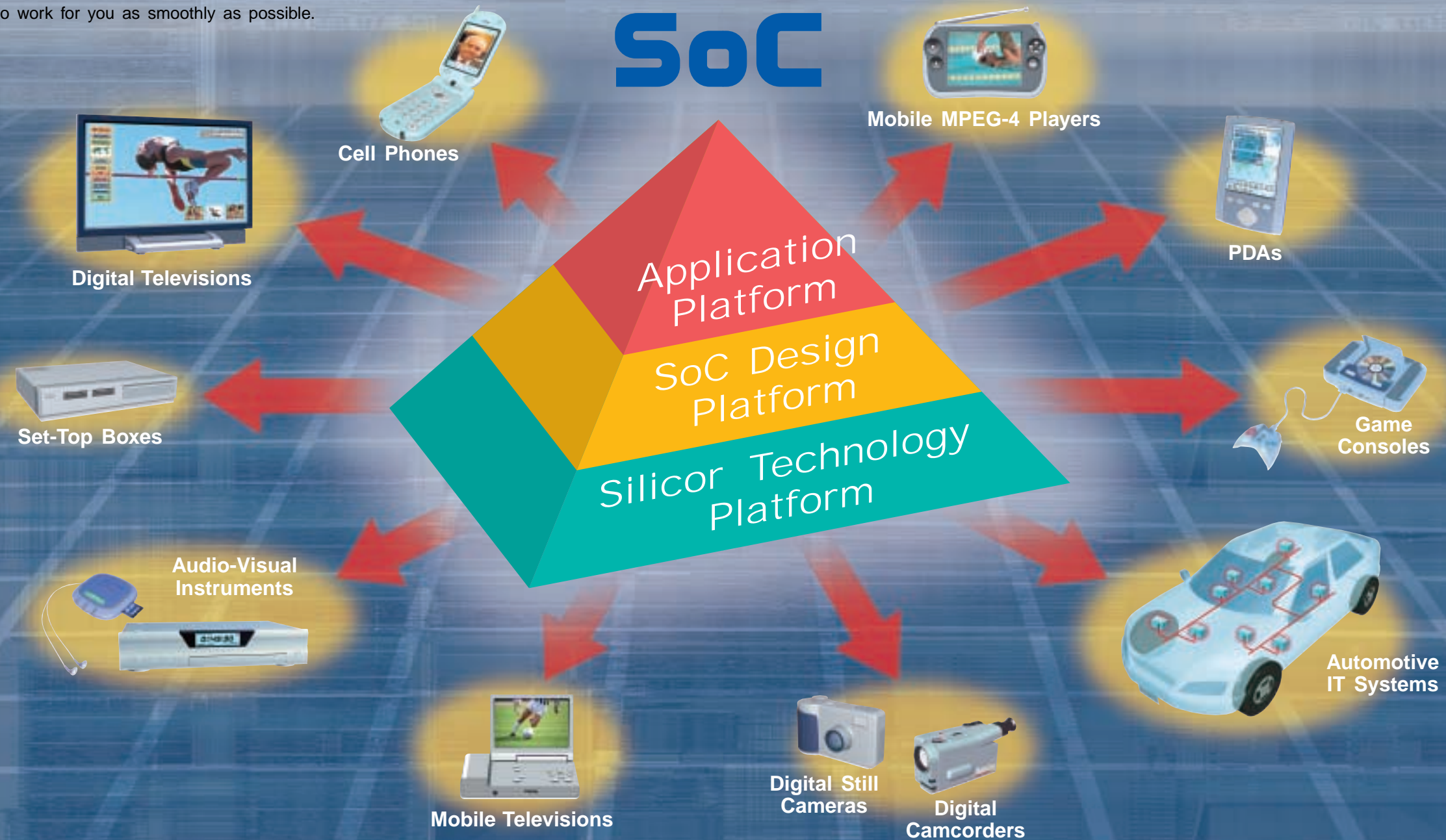
We believe that offering the best silicon capability is not enough and that it

is equally important to offer tools and methodologies so you can put our

world-class silicon capability to work for you as smoothly as possible.

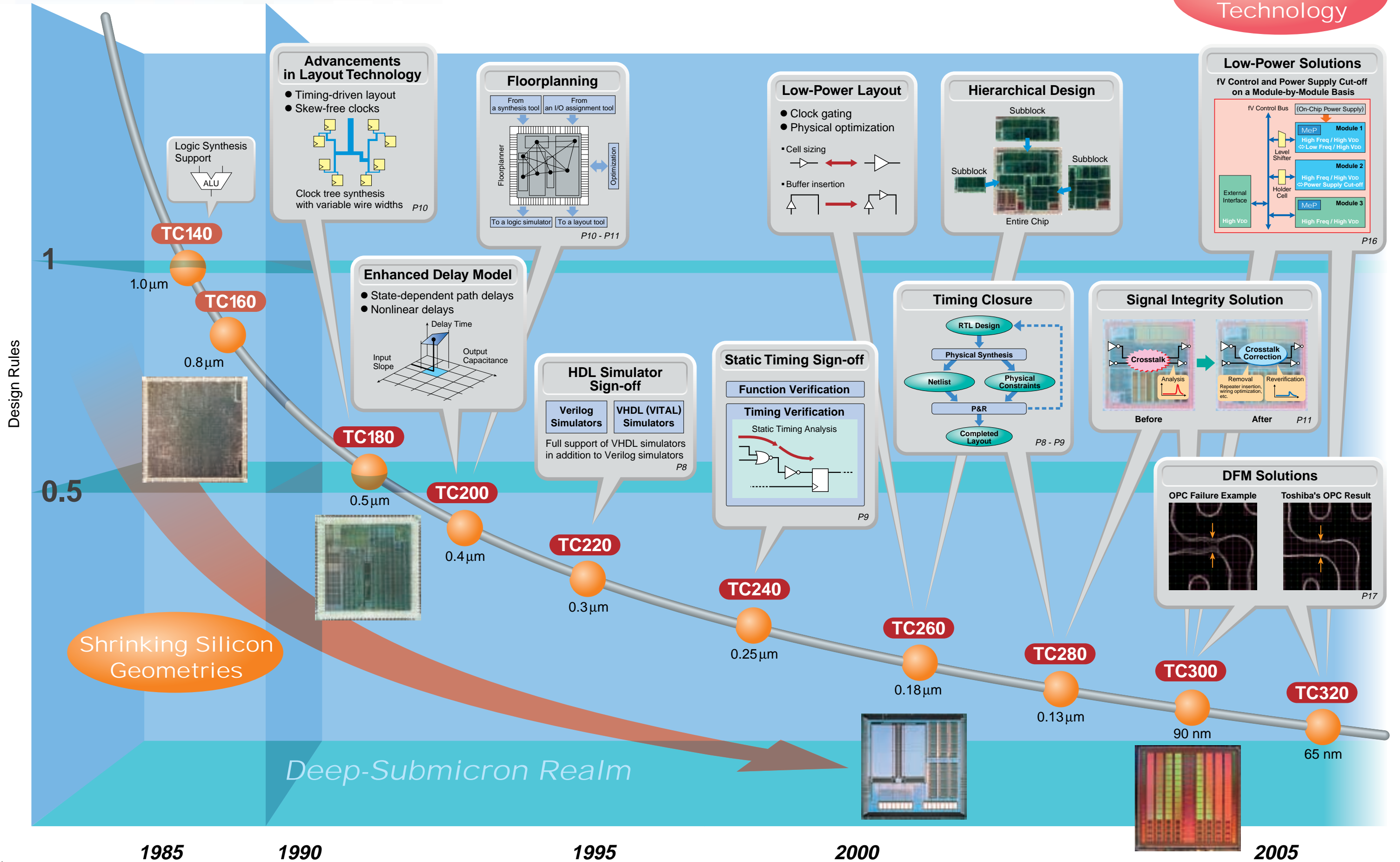
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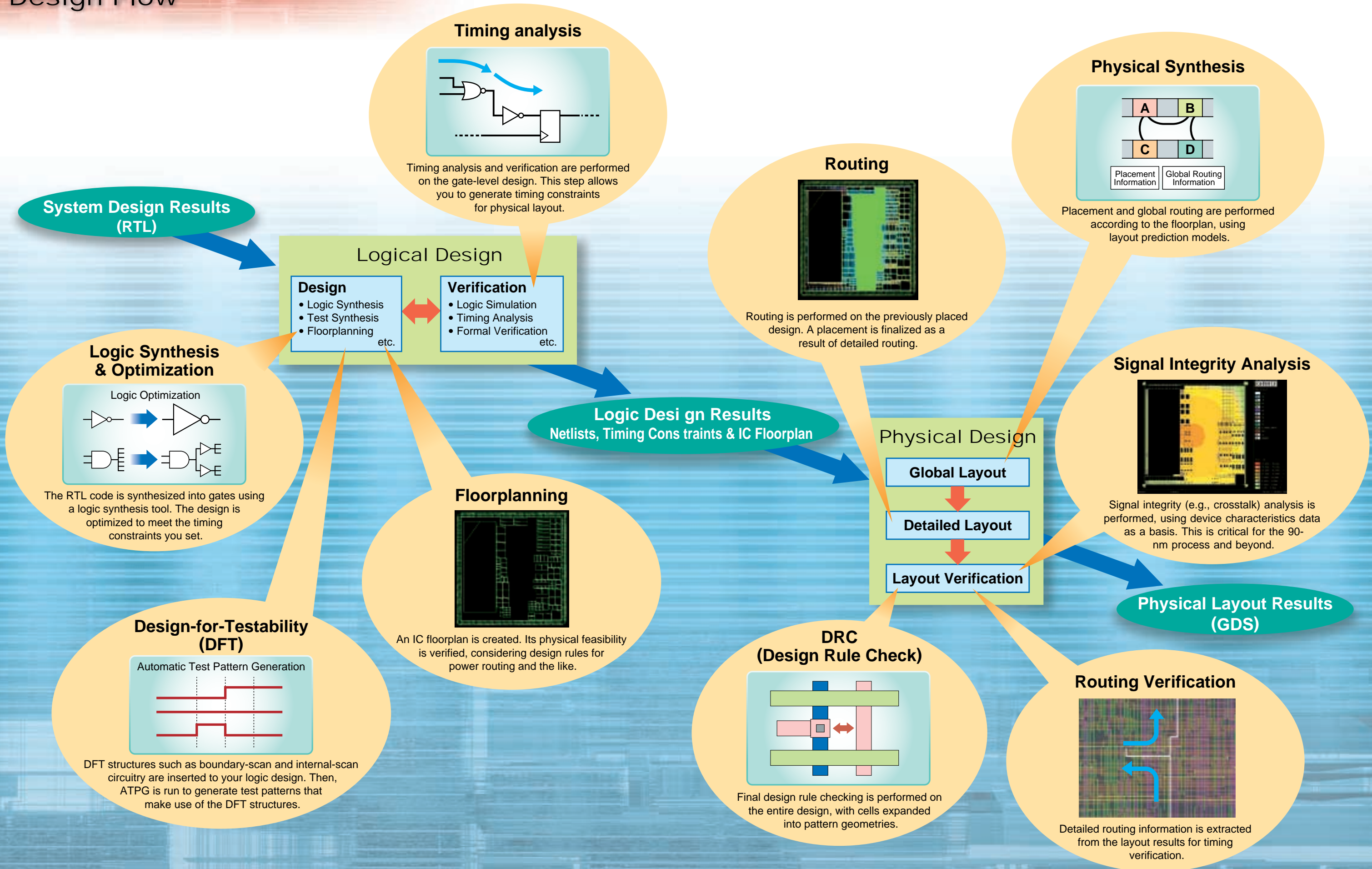


Toshiba's Evolving SoC EDA Solutions

Evolving EDA Technology



Design Flow

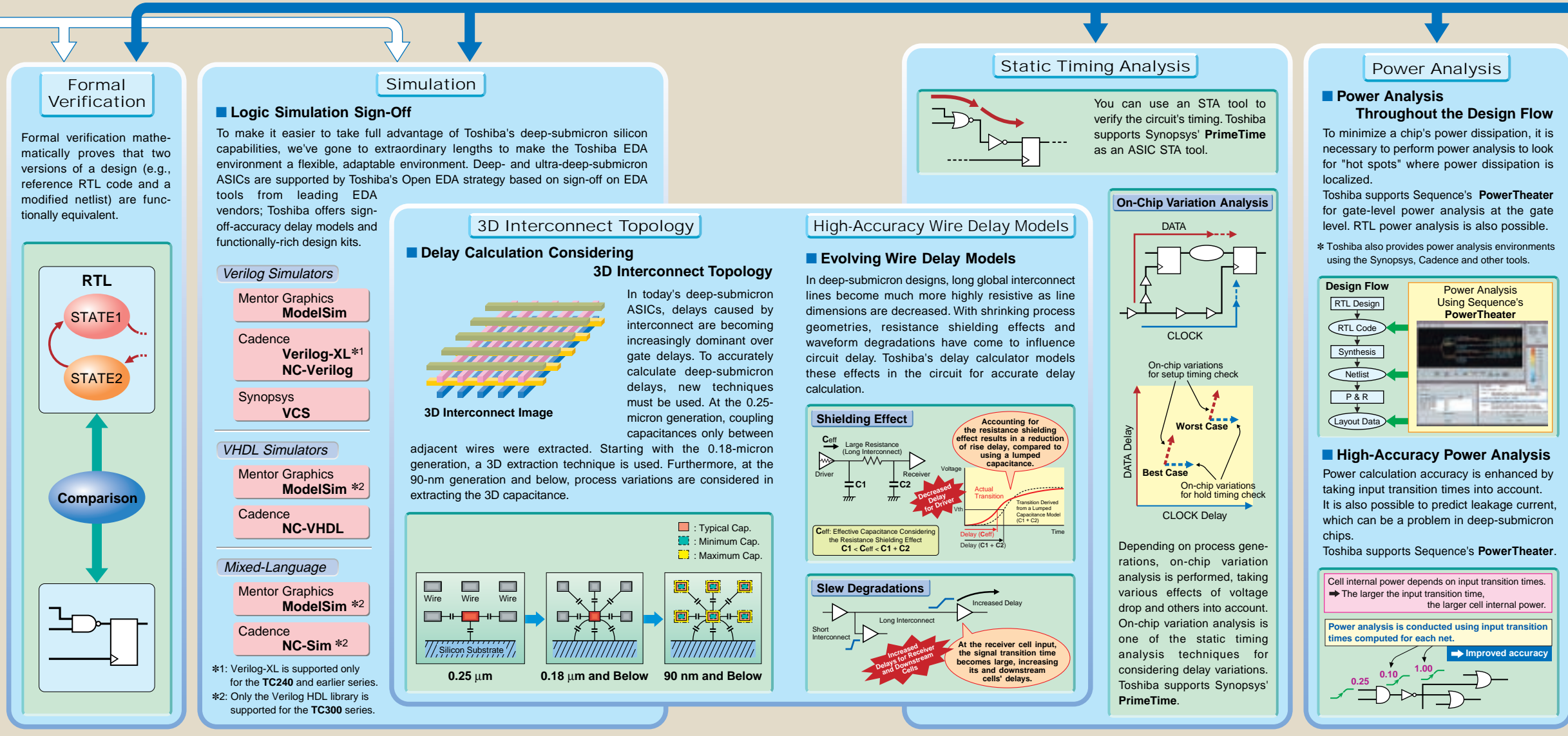


Design Environment: Logic Design Verification

There are two broad categories of design tools used after RTL verification: verification tools and implementation tools.

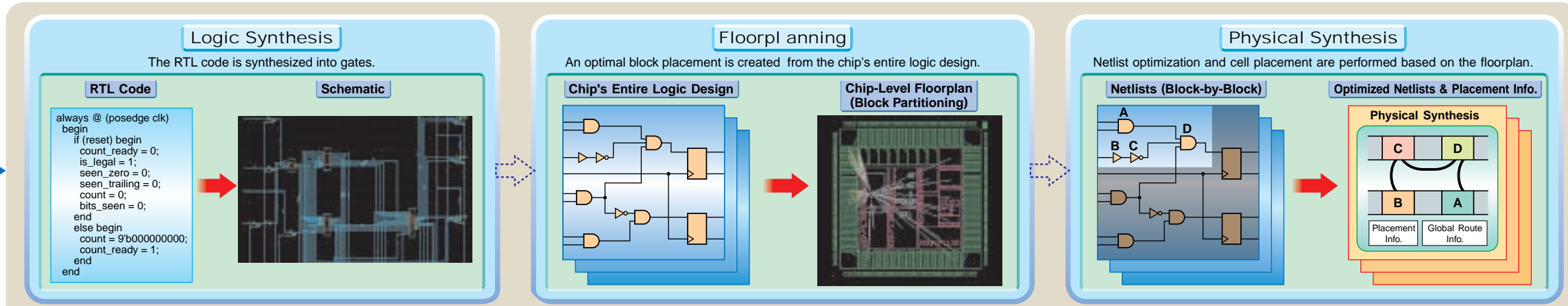
Verification Tools

Various kinds of verification and analysis are performed according to the needs of your SoC. We offer robust static timing analysis (STA) and simulation sign-off methodologies.



RTL, etc.

Netlist, etc.



These steps provide a bridge between RTL and physical design processes.

Implementation Tools

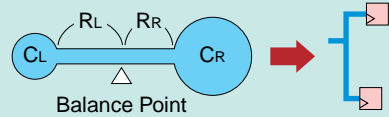
Design Environment: Physical Layout

Clock Skew Management

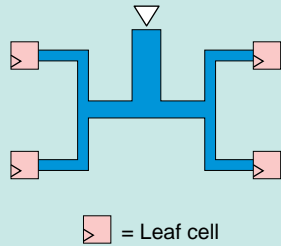
Toshiba's clock tree synthesis tool (TCTS) minimizes on-chip clock skew by balancing all cells within each net and using variable wire widths. TCTS not only realizes skew-free clocks, but also cuts clock insertion delay and fixes electromigration violations.

Automatic Skew-Free Clock Routing

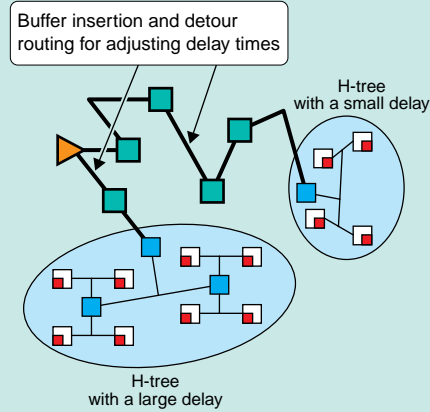
RC Delay Balancing



Variable Wire Widths



Skew Minimization

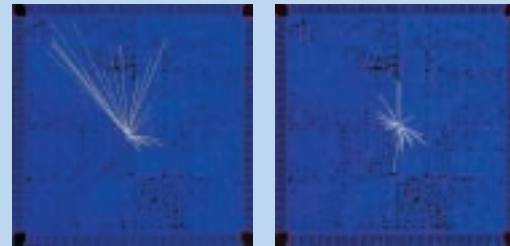


- Skew-free
- Supports clock gating and assures signal integrity.
- Electromigration analysis and correction

Timing Optimization

Timing constraints used for synthesis are passed to the layout tool to drive placement and routing. This capability helps to reduce the number of iterations between synthesis and layout, resulting in a dramatic reduction in the overall design time.

Timing-Driven Layout

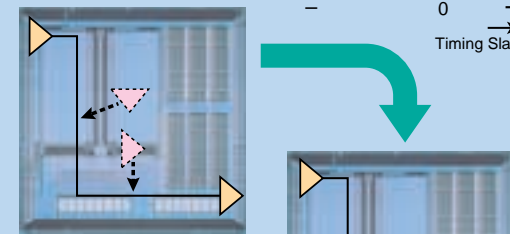
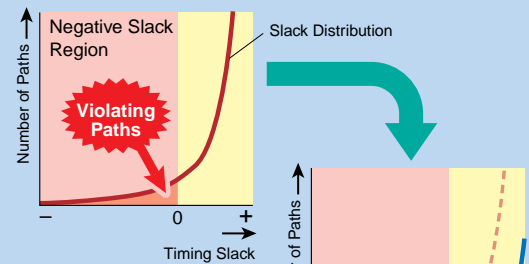


Timing Assurance Disabled Timing Assurance Enabled

This shows that the timing-driven placement run placed related cells closer together.

Repeater Insertion

The tool automatically determines where to insert repeaters, based on the results of global routing. The purpose of repeater insertion is twofold: reduction of interconnect delay and electro-migration correction.



Before Repeater Insertion

After Repeater Insertion

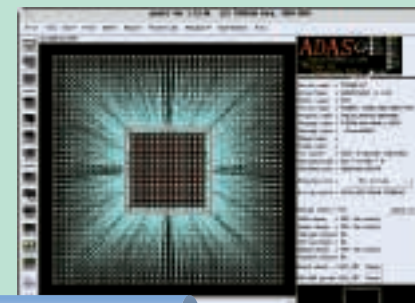
Chip Size Estimation

Toshiba's CSE (Chip Size Estimator) is used to estimate the size of the chip, based on an initial design specification.



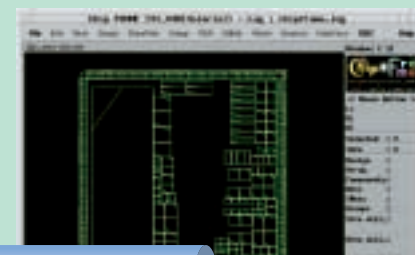
Packaging Interface

Toshiba's ADAS (Advanced Design & Assembly System) is a chip-to-package interconnection tool with a flip-chip BGA capability. ADAS automatically places I/O cells, inserts power/ground cells, creates bonding wire connections and so forth.



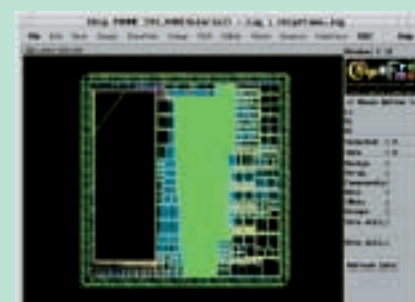
Floorplanning

Toshiba's ChipFrame is used to create an IC floorplan and perform preprocessing steps necessary prior to place-and-route.



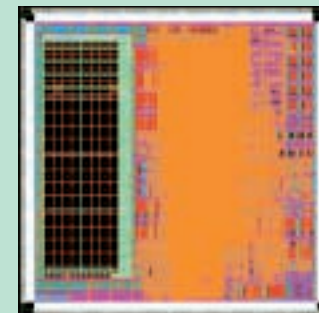
Place-and-Route

During the place-and-route phase, Toshiba's unique tools and methodologies are employed to improve timing, resolve signal integrity problems, address design-for-manufacturability (DFM) issues and perform various verification and optimization tasks.



GDS

The final chip design is written out in the GDS format. Upon final validation, the circuit is released to manufacturing.

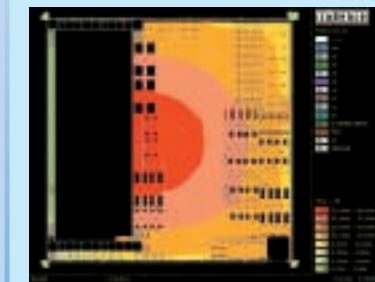


Signal Integrity

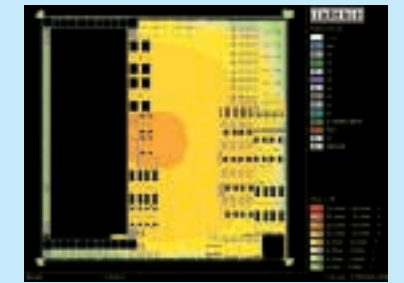
Voltage Drop Analysis and Prevention

As process geometry decreases and power supply voltage lowers, supply voltage drop problems are exacerbated, resulting in sub-optimal chip performance. At Toshiba, we estimate voltage drop value at early design stages and implement various novel techniques to prevent them, such as optimizing power grid routing and comprehensively reducing chip's power dissipation.

Even if the voltage does drop, we consider the impact of the voltage drop as a margin of a timing analysis.



Before



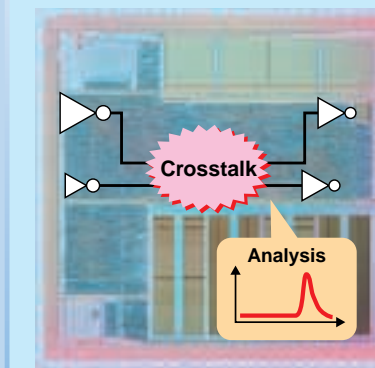
After

* These are graphical plot outputs from the Cadence VoltageStorm.

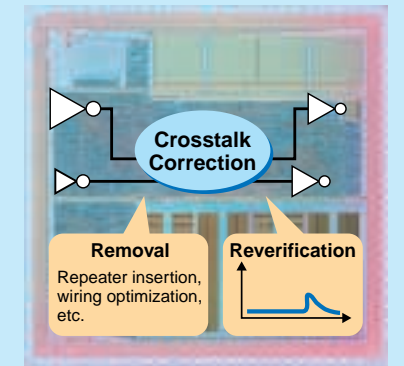
Crosstalk Analysis and Prevention

Crosstalk is a pressing SI-related issue which causes device function failures and unpredictable delay side effects.

The crosstalk prevention, analysis and removal features are integrated into the Toshiba design flow.



Before



After

Design Environment: Co-verification

Hardware/Software Co-verification

The traditional approach to the development of a system-on-a-chip (SoC) containing a CPU core is usually a series of sequential and independent steps, fragmented into task-oriented specialties. This significantly degrades design and design-change productivity. Hardware/software (HW/SW) co-verification provides an efficient solution to an SoC design with an embedded CPU core.

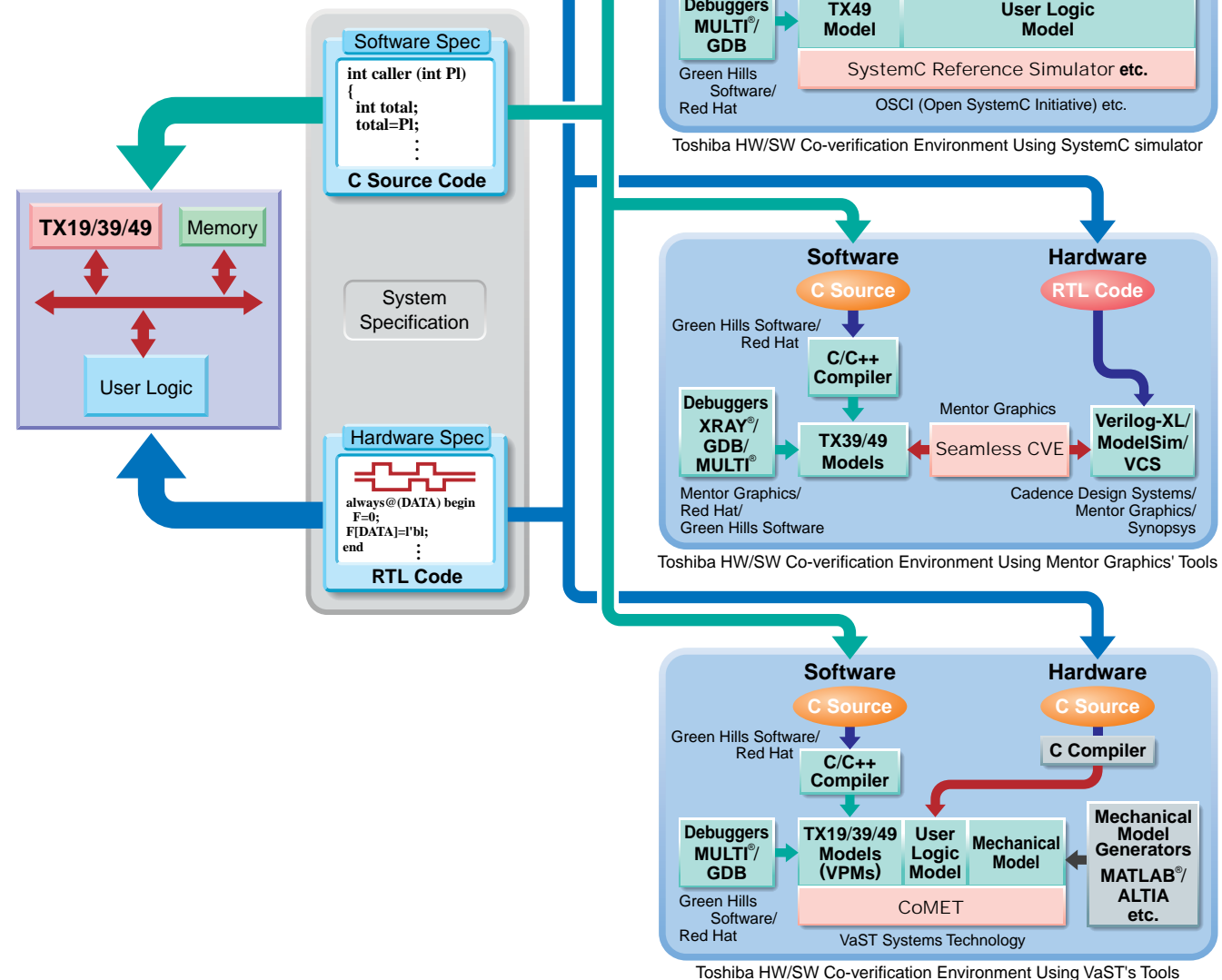
For hardware engineers, Toshiba supports SystemC simulator from OSCI and Seamless CVE from Mentor Graphics Corp. Toshiba provides **TX49 C** model of for SystemC simulator and the **TX39** and **TX49 C** models for Seamless CVE.

For software engineers, Toshiba supports CoMET from Vast Systems Technology Corp, which provides Virtual Processor Models (VPMs) of the **TX19**, **TX39** and **TX49**.

SystemC simulator is a high-performance and high-accuracy all-SystemC co-verification tool, which allows you to integrate user logic modeled in SystemC and the **TX49 C** model with a SystemC wrapper.

Seamless CVE is a high-accuracy co-verification environment that allows logic simulation of the user logic and debugging of device driver software using the **TX39** or **TX49 C** models.

CoMET features execution speed close to an actual hardware prototype and provides an ability to run full systems including real-time operating system (RTOS) and application software. It allows you to integrate the C model of the user logic and the VPM of **TX19**, **TX39** or **TX49**.



Design Environment: Design-for-Testability (DFT)

Design-for-Testability (DFT) Techniques

Design Environments and Methodology to Generate High-Quality Test Patterns

To minimize the probability that defective chips are shipped, high-quality manufacturing test patterns are required. Toshiba supports popular design-for-testability (DFT) techniques such as internal-scan to help you facilitate test pattern development. You can choose how much of the DFT task you want to do yourself. If you have your own DFT tool, you can perform the entire DFT task at your site. Alternatively, you can entrust the DFT task to Toshiba, provided you create your design in compliance with test design rules.

Supported DFT Techniques

JTAG Boundary-Scan Design

JTAG boundary-scan is the most widely used board-level test vehicle defined by IEEE Std. 1149.1. Toshiba's ASIC cell offerings include a complete set of boundary-scan register (BSR) cells and several JTAG controllers.

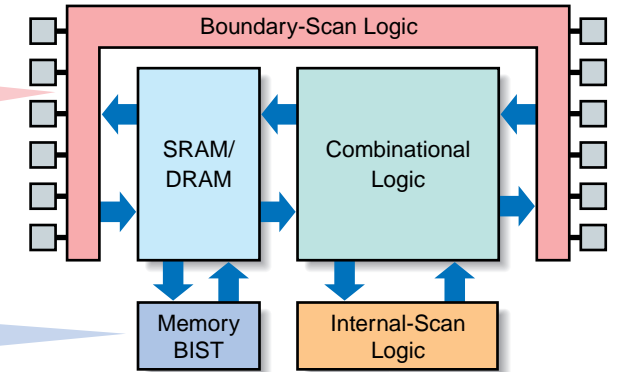
Memory BIST Design

Toshiba offers a design environment to automatically insert BIST logic for on-chip SRAMs and mask ROMs.

- Features: 1) Supports concurrent testing of multiple RAMs.
- 2) Generates compact BIST logic at RTL.
- 3) Automatically inserts the BIST logic to your design.
- 4) Uses a robust test algorithm called March 13N with two data backgrounds.
- 5) Allows you to freely specify the operating speed of BIST logic.

Toshiba inserts BIST logic for DRAMs for you.

- Features: 1) Supports concurrent testing of multiple DRAM macros.
- 2) Allows you to specify various test conditions.



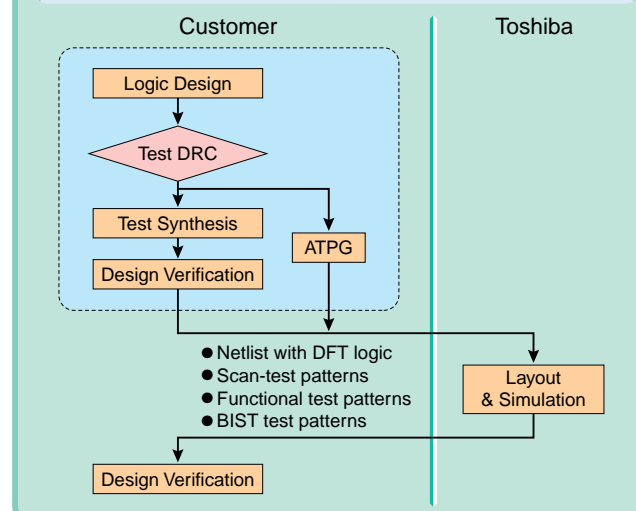
Internal-Scan Design

Internal-scan transforms a design in a manner to enable automatic test pattern generation for combinational circuits. There are two categories of scan flip-flops from which you can select to implement internal-scan: area-oriented flip-flops and speed-oriented flip-flops.

When customers perform the DFT task using commercially available third-party tools and Toshiba's design kits

DFT Design Environment

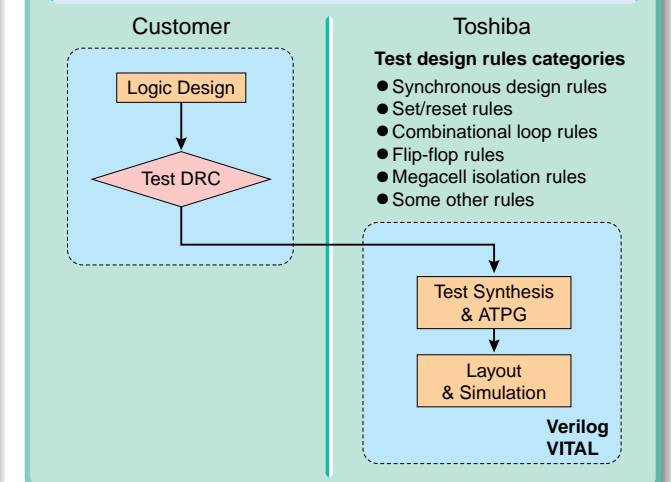
- Synopsys DFT Compiler, TetraMAX, BSD Compiler : Internal-scan, compressed-scan + ATPG, JTAG boundary-scan
- Mentor Graphics DFTAdvisor, FastScan : Internal-scan + ATPG
- Automatic memory BIST tools



When Toshiba performs the DFT task

DFT Design Environment

- Toshiba VSO/DFT, VITALSO/DFT : Test design rules checking, Internal-scan + ATPG, JTAG boundary-scan
- Synopsys DFT Compiler, TetraMAX, BSD Compiler : Internal-scan, compressed-scan + ATPG, JTAG boundary-scan
- Automatic memory BIST tools



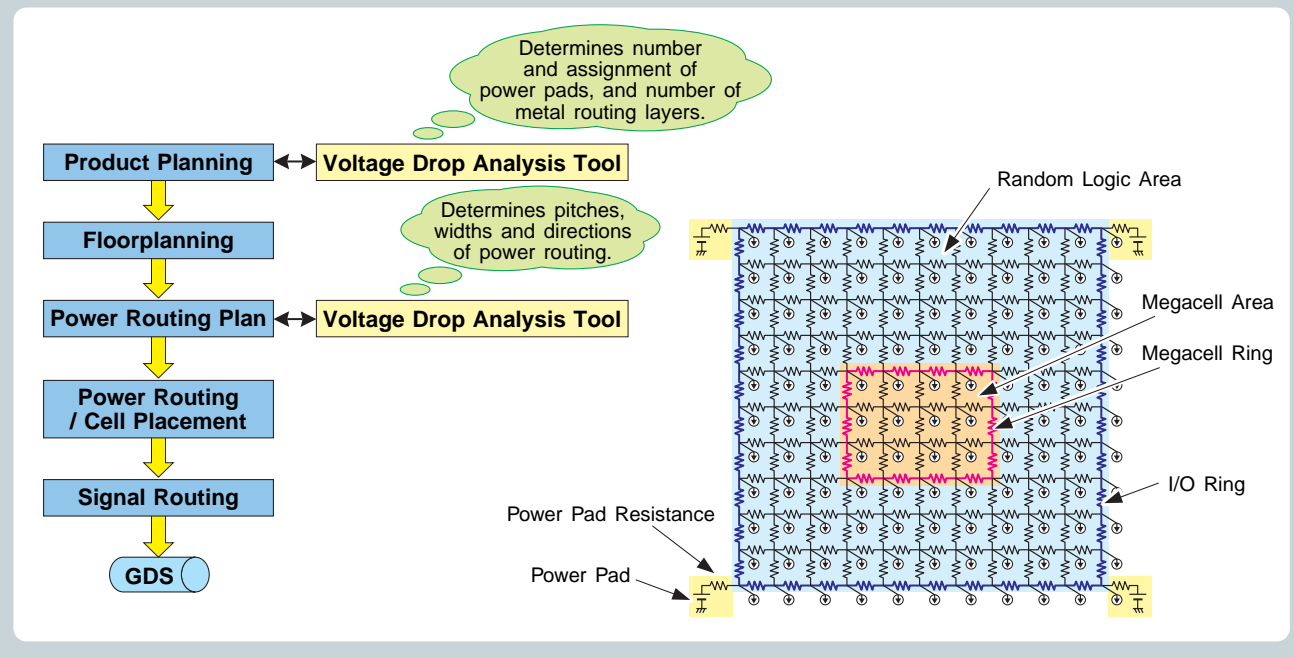
Design Environment: High-Quality Designs

Enhanced Signal Integrity Solutions

Signal integrity (SI) problems such as crosstalk and voltage drop have emerged as a first-order design issue that can cause functional failures. Followings are brief descriptions of the techniques Toshiba uses for voltage drop analysis. Particularly, quick voltage drop analysis during floorplanning is realized by Toshiba's original tool.

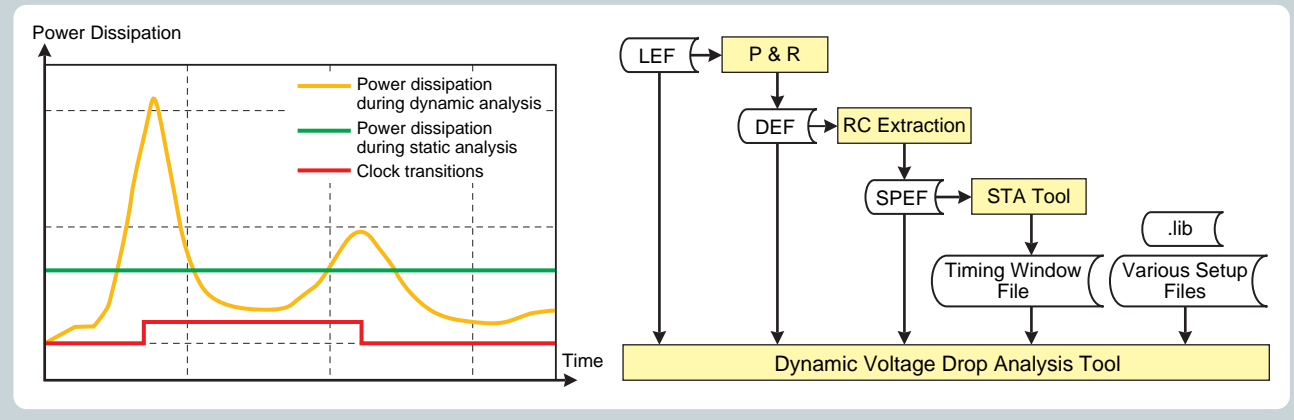
Quick Voltage Drop Analysis During Floorplanning

As a design goes through the physical layout flow, it becomes more difficult to correct voltage drop errors. It is important to implement voltage drop prevention as early as possible in the design cycle. At Toshiba, we generate a rough power grid model from a power routing plan and statically analyze voltage drop during floorplanning. This technique can take the pad assignment and floorplan into account and allows quick and accurate voltage drop prediction prior to actual power routing.



Dynamic Voltage Drop Analysis

Dynamic voltage drop (power noise) means a temporal change of the power supply voltage at various locations within the design. While static voltage drop is based on the circuit's average power dissipation during a given period, dynamic voltage drop is thought to spike momentarily to a level a few times greater than static voltage drop, because dynamic voltage drop is especially affected by clock transitions. There is a concern that such abrupt voltage drop might influence cell performance. A design flow with a dynamic voltage drop analysis tool addresses this problem.

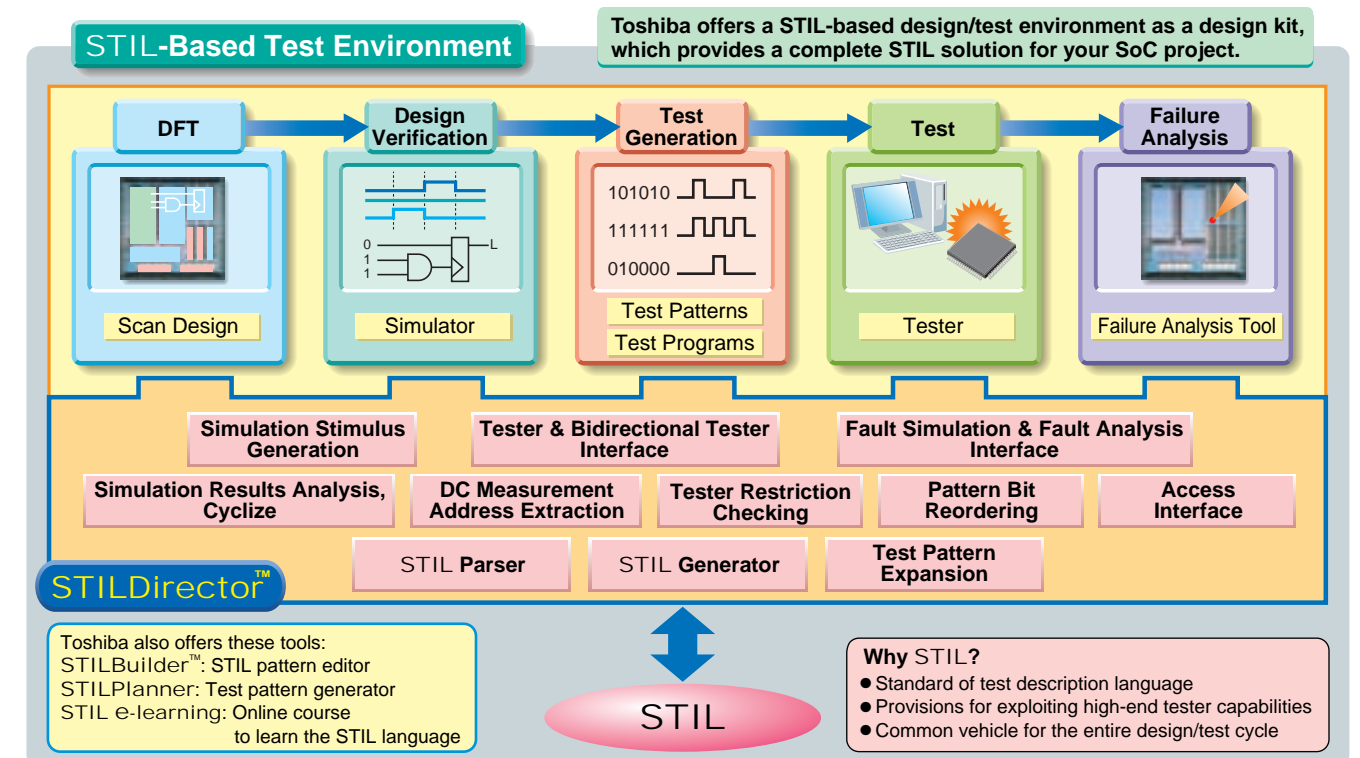


Design Environment: System Solutions

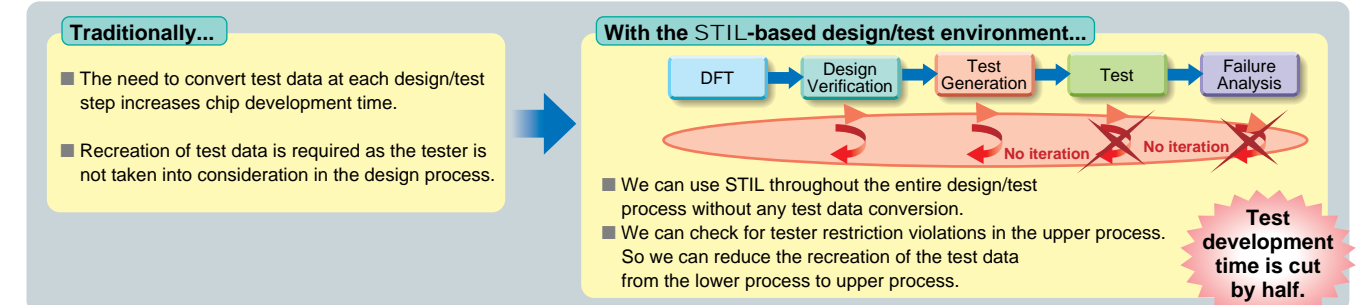
STIL-Based SoC Test Solutions

We provide you the design/test environment conforming to the international standard test description language STIL^(*). We can use STIL output by Automatic Test Pattern Generation tool (ATPG), STIL generated by Simulator, and STIL supplied by IP vendor. So it is possible to use the test data efficiently. Therefore we can shorten the test data generation time, and we can reduce the test cost. Additionally we can shorten TAT from Design to Test and Failure Analysis by handling test data of each step with STIL.

(*STIL (Standard Test Interface Language) is test data description language approved as IEEE std 1450-1999. STIL reads "style")

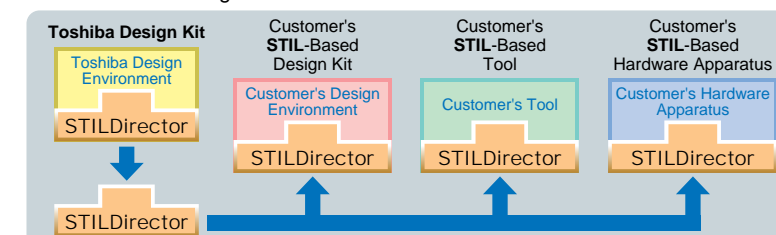


Benefits of the STIL-Based Design/Test Environment



STILDirector™: STIL Open Plug-In System

To let you quickly build a STIL-based design/test environment at a low cost, Toshiba offers an open plug-in system called STILDirector, which is a subset of the Toshiba design kit.



Benefits of Using STIL

- Facilitates test data interface among EDA tools and test equipment.
- Offers greater flexibility in test descriptions, making it possible to exploit the tester capabilities. (Complex timing descriptions, effective use of tester's pattern memory, etc.)
- Provides a standard means of exchanging test data for IP cores.
- Allows for the representations of complicated tests. (e.g., scan information and other DFT features)

* STILDirector and STILBuilder are trademarks of Toshiba Microelectronics Corporation.

Solution for Next-Generation

Design environments for the 90-nm node are almost complete. While the 90-nm node poses significant design difficulties, the 65-nm node requires a range of new and enhanced technologies to ensure your design success. Toshiba is working on those outlined here.

Low-Power Solutions

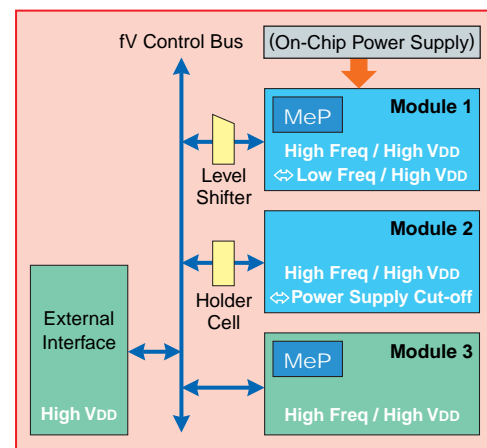
As processes move into nanometer feature sizes, power dissipation due to leakage current is rapidly increasing. To minimize leakage current during standby, Toshiba offers power supply cut-off and selective-MT techniques. To reduce dynamic current, Toshiba offers fV control feature.

fV Control

The fV control technique allows optimum control of frequencies and power supply voltages on a module-by-module basis to reduce switching and leakage current during active operation.

- Toshiba is now developing a tool to insert level shifters and holder cells automatically, as well as the fV control bus, multi-condition libraries and on-chip power supply macros.
- For example, with high $V_{DD} = 1.2\text{ V}$ and low $V_{DD} = 0.9\text{ V}$, the fV control technology will offer you a power reduction of up to 40%.

fV Control and Power Supply Cut-off on a Module-by-Module Basis



Toshiba's Low-Power Solutions

	Standby	Active
Dynamic		Gated clocks Conditional flip-flops fV control
Leakage	Multi-Vt Power supply cut-off Selective-MT Low-leakage SRAM	Multi-Vt fV control Block power supply cut-off Low-leakage SRAM

Available with the MeP platform

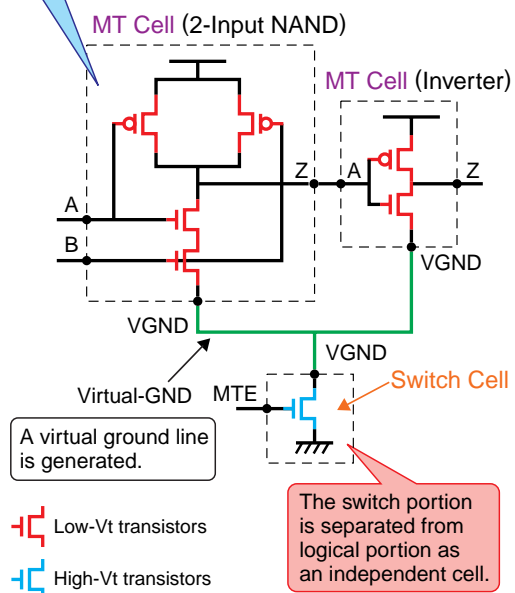
Selective-MT Technique

While Toshiba had been offering a Selective-MT technique to realize ultra-low standby leakage current, the traditional technique has been improved on the following point.

A single switch cell can be shared among multiple MT cells.

- Shared switch cells result in reduced chip area.
- Standby leakage current is cut by up to 90%, compared to the multi-Vt technique.

Switch and output holder portions were separated from the MT cell.

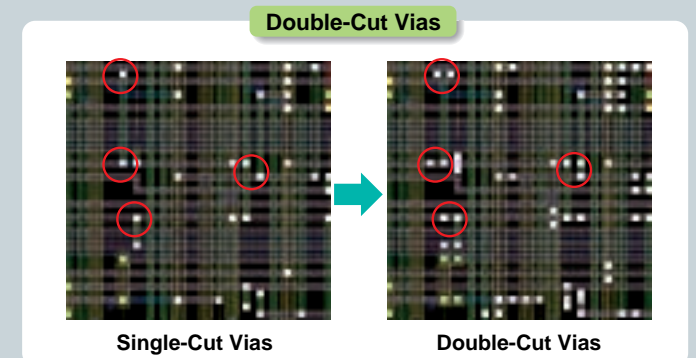


DFM Solutions

The patterning resolution of lithography has not been able to keep pace with rapidly shrinking device geometries. Toshiba addresses such problems by using design-for-manufacture (DFM) from early in the design cycle.

Yield Improvement

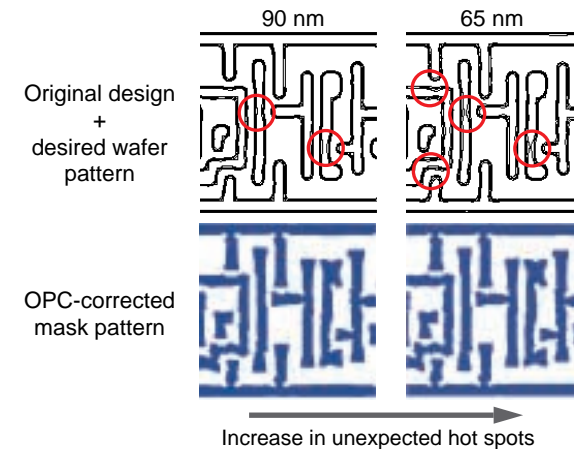
Traditionally, single cut vias were used for routing random logic regions. Double cut vias can now be applied to improve manufacturing yield. The screen shot at right shows an example of routing using double cut vias. Also, wire spreading is used to reduce routing congestion to minimize opens and shorts during manufacturing due to dust particles.



Lithography Considerations

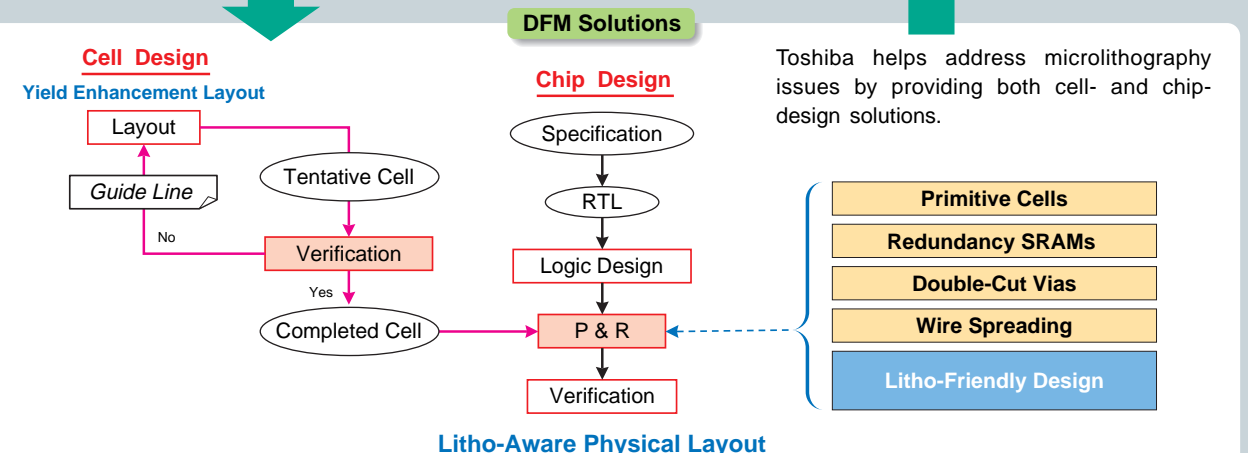
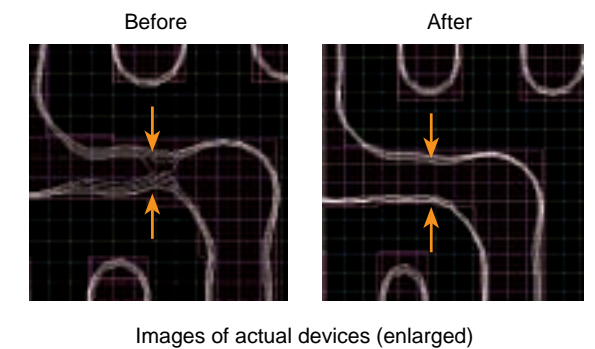
Problem

– Lowering image fidelity due to reduced feature sizes –



Results

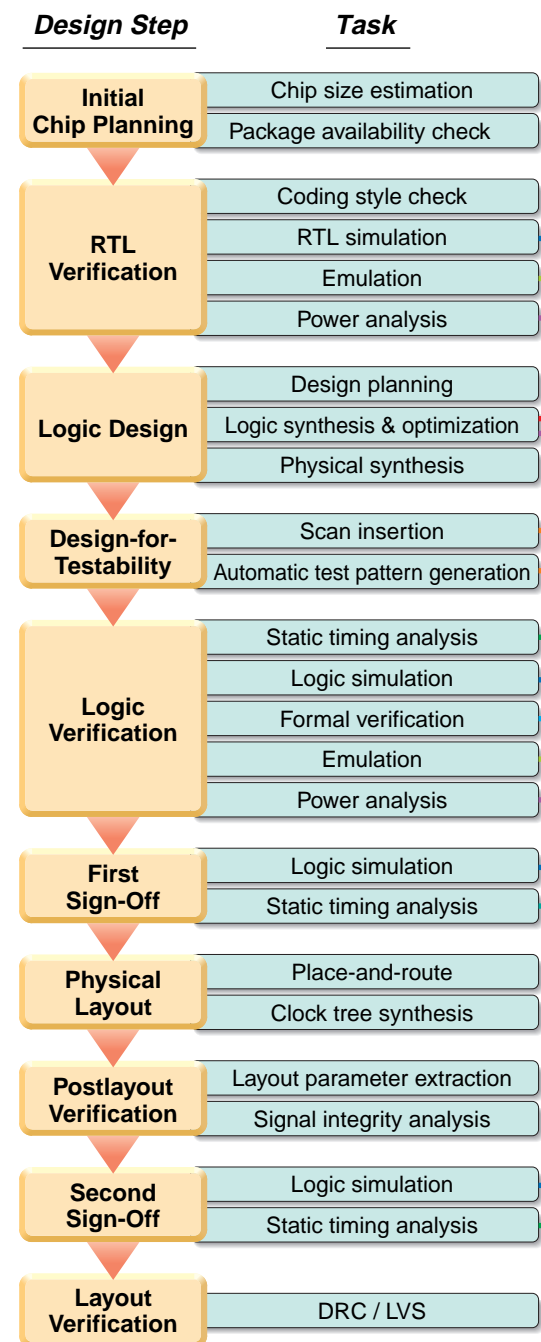
– Improvement example by DFM solution –



Toshiba helps address microlithography issues by providing both cell- and chip-design solutions.

Design Kit Support

Typical Design Flow



Supported EDA Tools and Design Kit Availability

ASIC Product Family		Cell-Based ICs										Gate Arrays					Embedded Arrays				
		TC 300C ^{*1}	TC 280C ^{*1}	TC 260C	TC 223C	TC 222C	TC 220C	TC 203C	TC 200C	TC 190C	TC 223G	TC 220G	TC 203G	TC 200G	TC 190G	TC 260E	TC 223E	TC 220E	TC 203E	TC 200E	
EDA Tool	Logic Synthesis Tools	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	Design Compiler	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
Simulators	Verilog-XL	—	—	—	●	●	●	●	●	●	●	●	●	●	—	●	●	●	●	●	
	VCS	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	NC-Verilog	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	NC-Sim	● ^{*2}	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	ModelSim	● ^{*2}	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	NC-VHDL	—	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
Static Timing Analysis Tools	PrimeTime	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	Formal Verification Tools	●	●	●	—	—	—	—	—	—	—	—	—	—	—	●	—	—	—	—	
DFT Tools	Formality	●	●	●	—	—	—	—	—	—	—	—	—	—	●	—	—	—	—		
	Conformal LEC	●	●	●	—	—	—	—	—	—	—	—	—	—	●	—	—	—	—		
	DFT Compiler / BSD Compiler	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
Power Analysis and Optimization	DFTAdvisor / FastScan	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	TetraMAX	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
Emulators	Power Theater	●	●	●	—	—	—	—	—	—	—	—	—	—	●	—	—	—	—		
	Celaro	●	●	●	—	—	—	—	—	—	—	—	—	—	●	—	—	—	—		

The above table shows the basic cell availability status. For availability of megacells such as RAMs and ROMs, ask the nearest Toshiba ASIC design center. Please obtain the latest technical material before you begin creating a design.

*1: TC300C and TC280C optionally provide a cell-based IC option called **UniversalArray™**, a tool specifically designed to reduce development time.
 *2: The ModelSim and NC-Sim libraries for the TC300C series support only Verilog HDL.

Trademarks

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**Toshiba America
Electronic Components, Inc.**

Headquarters-Irvine, CA
19900 MacArthur Boulevard,
Suite 400, Irvine, CA 92612, U.S.A.
Tel: (949)623-2900 Fax: (949)474-1330

Boulder, CO (Denver)
3100 Arapahoe #500,
Boulder, CO 80303, U.S.A.
Tel: (303)442-3801 Fax: (303)442-7216

Buffalo Grove (Chicago)
2150 E. Lake Cook Road, Suite 310,
Buffalo Grove, IL 60089, U.S.A.
Tel: (847)484-2400 Fax: (847)541-7287

Duluth, GA (Atlanta)
3700 Crestwood Pkwy, #160,
Duluth, GA 30096, U.S.A.
Tel: (770)931-3363 Fax: (770)931-7602

Portland, OR
2560 NW 141st Place Portland,
OR 97229, U.S.A.
Tel: (503)784-8879 Fax: (503)466-9729

Raleigh, NC
3120 Highwoods Blvd., #108, Raleigh,
NC 27604, U.S.A.
Tel: (919)859-2800 Fax: (919)859-2898

Richardson, TX (Dallas)
777 East Campbell Rd., #650, Richardson,
TX 75081, U.S.A.
Tel: (972)480-0470 Fax: (972)235-4114

San Jose Engineering Center, CA
2590 Orchard Parkway San Jose,
CA 95131, U.S.A.
Tel: (408)526-2400 Fax: (408)526-2410

Wakefield, MA (Boston)
401 Edgewater Place, #360, Wakefield,
MA 01880-6229, U.S.A.
Tel: (781)224-0074 Fax: (781)224-1095

Wixom (Detroit)
48679 Alpha Drive, Suite 100, Wixom,
MI 48393 U.S.A.
Tel: (248)449-6165 Fax: (248)449-8430

Toshiba Electronics do Brasil Ltda.
Rua Afonso Celso, 552-8 andar, CJ. 81
Vila Mariana Cep 04119-002 São Paulo SP, Brasil
Tel: (011)5576-6619 Fax: (011)5576-6607

Toshiba India Private Ltd.
6F DR. Gopal Das Bhawan 28,
Barakhamba Road, New Delhi, 110001, India
Tel: (011)2331-8422 Fax: (011)2371-4603

Toshiba Electronics Europe GmbH

Düsseldorf Head Office
Hansaallee 181, D-40549 Düsseldorf,
Germany
Tel: (0211)5296-0 Fax: (0211)5296-400

München Office
Büro München Hofmannstrasse 52,
D-81379, München, Germany
Tel: (089)748595-0 Fax: (089)748595-42

France Branch
Les Jardins du Golf 6 rue de Rome F-93561,
Rosny-Sous-Bois, Cedex, France
Tel: (1)48-12-48-12 Fax: (1)48-94-51-15

Italy Branch
Centro Direzionale Colleoni,
Palazzo Perseo 3,
I-20041 Agrate Brianza, (Milan), Italy
Tel: (039)68701 Fax: (039)6870205

Spain Branch
Parque Empresarial, San Fernando, Edificio Europa,
1ª Planta, E-28831 Madrid, Spain
Tel: (91)660-6798 Fax: (91)660-6799

U.K. Branch
Riverside Way, Camberley Surrey,
GU15 3YA, U.K.
Tel: (01276)69-4600 Fax: (01276)69-4800

Sweden Branch
Gustavslundsvägen 18, 5th Floor,
S-167 15 Bromma, Sweden
Tel: (08)704-0900 Fax: (08)80-8459

**Toshiba Electronics Asia
(Singapore) Pte. Ltd.**
438B Alexandra Road, #06-08/12 Alexandra
Technopark, Singapore 119968
Tel: (6278)5252 Fax: (6271)5155

**Toshiba Electronics Service
(Thailand) Co., Ltd.**
135 Moo 5, Bangkok Industrial Park, Tivanon Road,
Pathumthani, 12000, Thailand
Tel: (02)501-1635 Fax: (02)501-1638

**Toshiba Electronics Trading
(Malaysia) Sdn. Bhd.**

Kuala Lumpur Head Office
Suite W1203, Wisma Consplant, No.2,
Jalan SS 16/4, Subang Jaya, 47500 Petaling Jaya,
Selangor Darul Ehsan, Malaysia
Tel: (03)5631-6311 Fax: (03)5631-6307

Penang Office
Suite 13-1, 13th Floor, Menara Penang Garden,
42-A, Jalan Sultan Ahmad Shah,
10050 Penang, Malaysia
Tel: (04)226-8523 Fax: (04)226-8515

Toshiba Electronics Philippines, Inc.
26th Floor, Citibank Tower, Valero Street, Makati,
Manila, Philippines
Tel: (02)750-5510 Fax: (02)750-5511

Toshiba Electronics Asia, Ltd.

Hong Kong Head Office
Level 11, Tower 2, Grand Century Place, No.193,
Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: 2375-6111 Fax: 2375-0969

Beijing Office
Room 714, Beijing Fortune Building, No.5 Dong San Huan Bei-Lu,
Chao Yang District, Beijing, 100004, China
Tel: (010)6590-8796 Fax: (010)6590-8791

Chengdu Office
Room 2508A, 2 Zongfu Street, Times Plaza,
Chengdu 610016 Sichuan, China
Tel: (028)8675-1773 Fax: (028)8675-1065

Qingdao Office
Room 4(D-E), 24F, International Financial Center,
59 Xiang Gang Zhong Road, Qingdao, Shandong, China
Tel: (0532)579-3328 Fax: (0532)579-3329

Toshiba Electronics Shenzhen Co., Ltd.
Room 2601-2609, 2616, Office Tower Shen Hing Square,
Di Wang Commercial Center, 5002 Shennan Road East,
Shenzhen, 518008, China
Tel: (0755)2583-0810 Fax: (0755)8246-1581

Toshiba Electronics (Shanghai) Co., Ltd.

Shanghai Head Office
11F, HSBC Tower, 1000 Lujiazui Ring Road,
Pudong New Area, Shanghai 200120, China
Tel: (021)6841-0666 Fax: (021)6841-5002

Hangzhou Office
502 JiaHua International Business Center,
No.28 HangDa Road, Hangzhou, 310007, China
Tel: (0571)8717-5004 Fax: (0571)8717-5013

Nanjing Office
23F Shangmao Century Plaza,
No.49 Zhong Shan South Road, Nanjing, 210005, China
Tel: (025)8689-0070 Fax: (025)8689-0125

Toshiba Electronics (Dalian) Co., Ltd.
14/F, Senmao Building, 147, Zhongshan Road,
Xigang Dist., Dalian, 116011, China
Tel: (0411)8368-6882 Fax: (0411)8369-0822

Tsurong Xiamen Xiangyu Trading Co., Ltd.
14G, International Bank BLDG., No.8 Lujiang Road,
Xiamen, 361001, China
Tel: (0592)226-1398 Fax: (0592)226-1399

Toshiba Electronics Korea Corporation

Seoul Head Office
891, Samsung Life Insurance Daechi Tower 20F, Daechi-dong,
Gangnam-gu, Seoul, 135-738, Korea
Tel: (02)3484-4334 Fax: (02)3484-4302

Gumi Office
6F, Goodmorning Securities Building, 56 Songjung-dong,
Gumi-shi, Gyeongbuk, 730-090, Korea
Tel: (054)456-7613 Fax: (054)456-7617

Toshiba Electronics Taiwan Corporation

Taipei Head Office
17F, Union Enterprise Plaza Building, 109
Min Sheng East Road, Section 3, Taipei, 10544, Taiwan
Tel: (02)2514-9988 Fax: (02)2514-7892

Kaohsiung Office
16F-A, Chung-Cheng Building, 2, Chung-Cheng 3Road,
Kaohsiung, 80027, Taiwan
Tel: (07)237-0826 Fax: (07)236-0046

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