

TOSHIBA

2007-3

Leading Innovation >>>

PRODUCT GUIDE

CMOS ASICs



To ensure competitiveness in the marketplace, you will need to produce more sophisticated, more technology-intensive and higher value-added products, using a process of technological innovation and systematic marketing. Toshiba's application-specific integrated circuits (ASICs) will give you an edge beyond your expectations. You can select from gate arrays, cell-based ICs and embedded arrays, depending on your performance and time-to-market objectives.

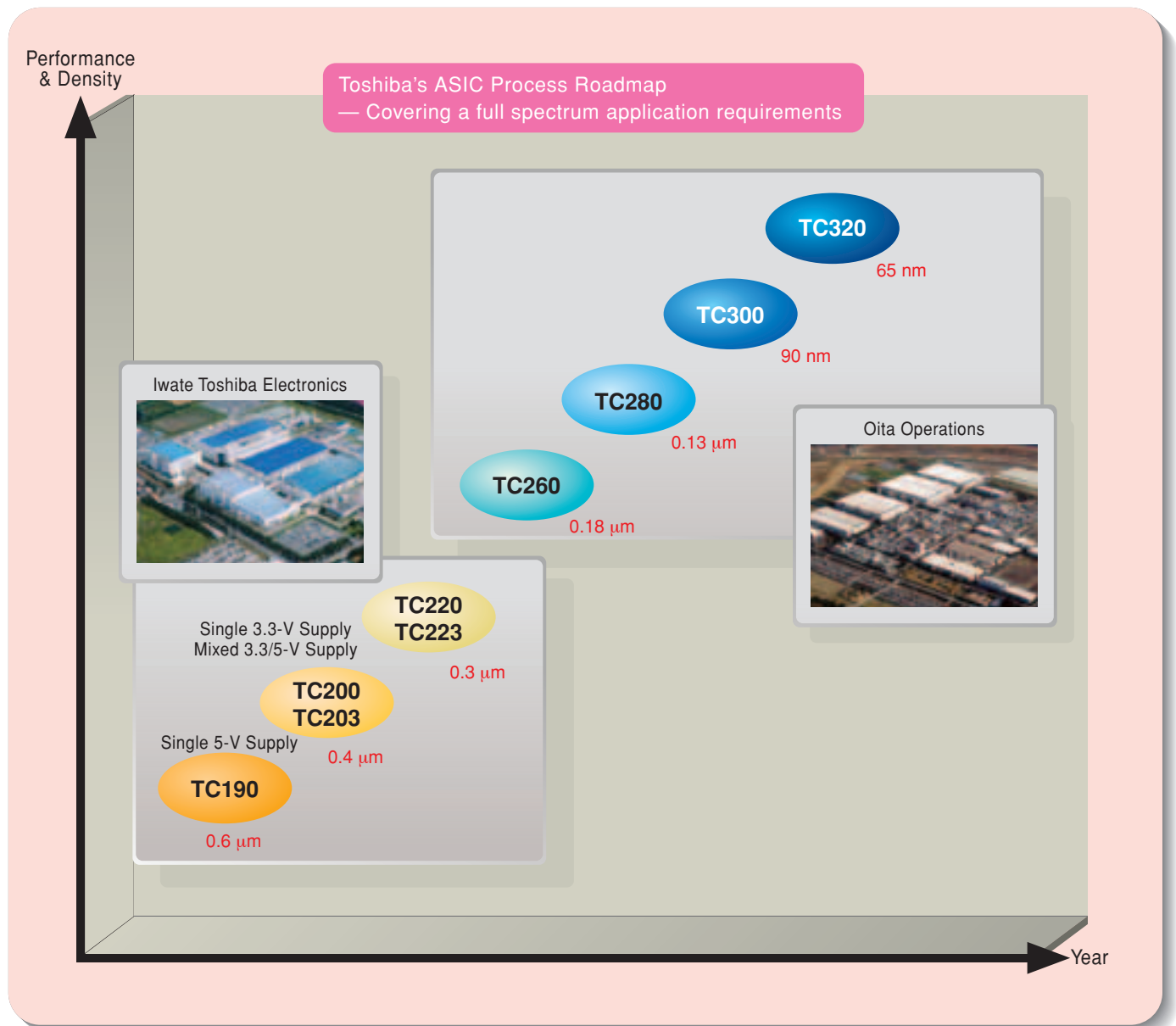
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System ASICs

Reuse of pre-designed and pre-verified IP cores offers the highest potential for improved design productivity and product performance. However, for the success of system ASICs, an extensive collection of IP cores must be supported by adequate silicon technologies and manufacturing capabilities.

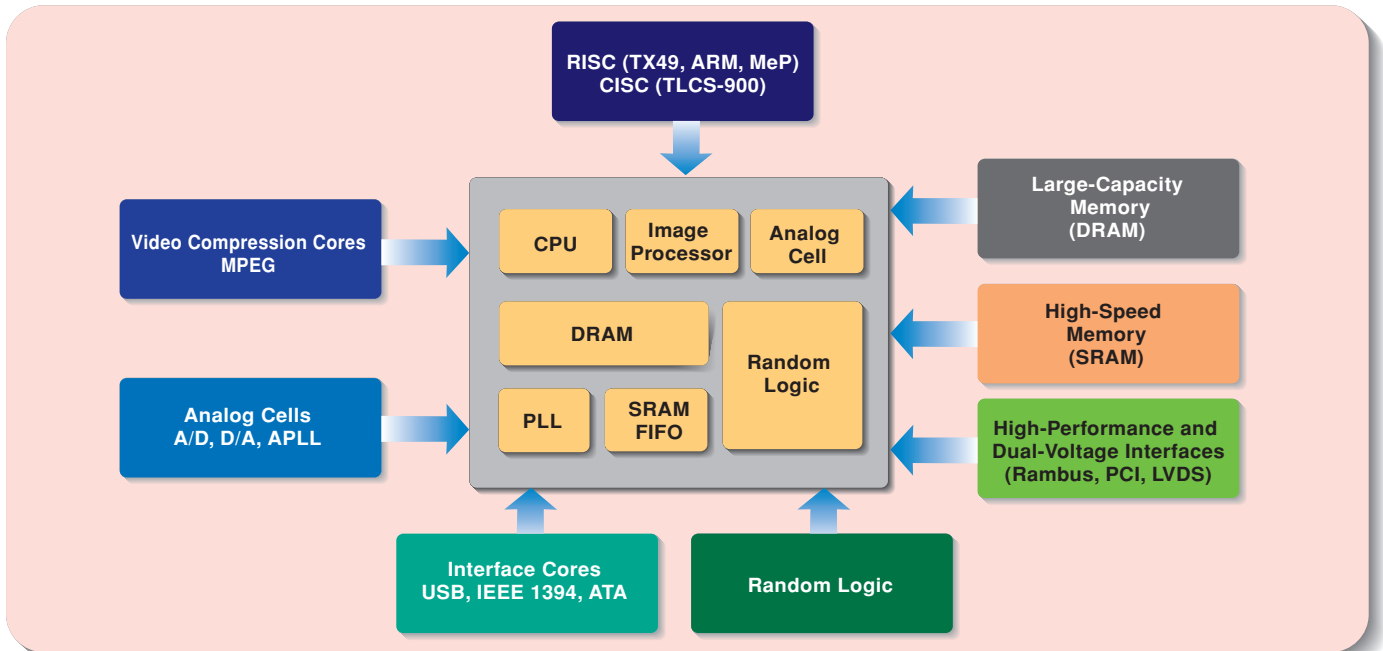
Toshiba continuously pursues new goals in the exploration of system ASICs with a broad range of power, density and speed solutions, complete with support of core functions.



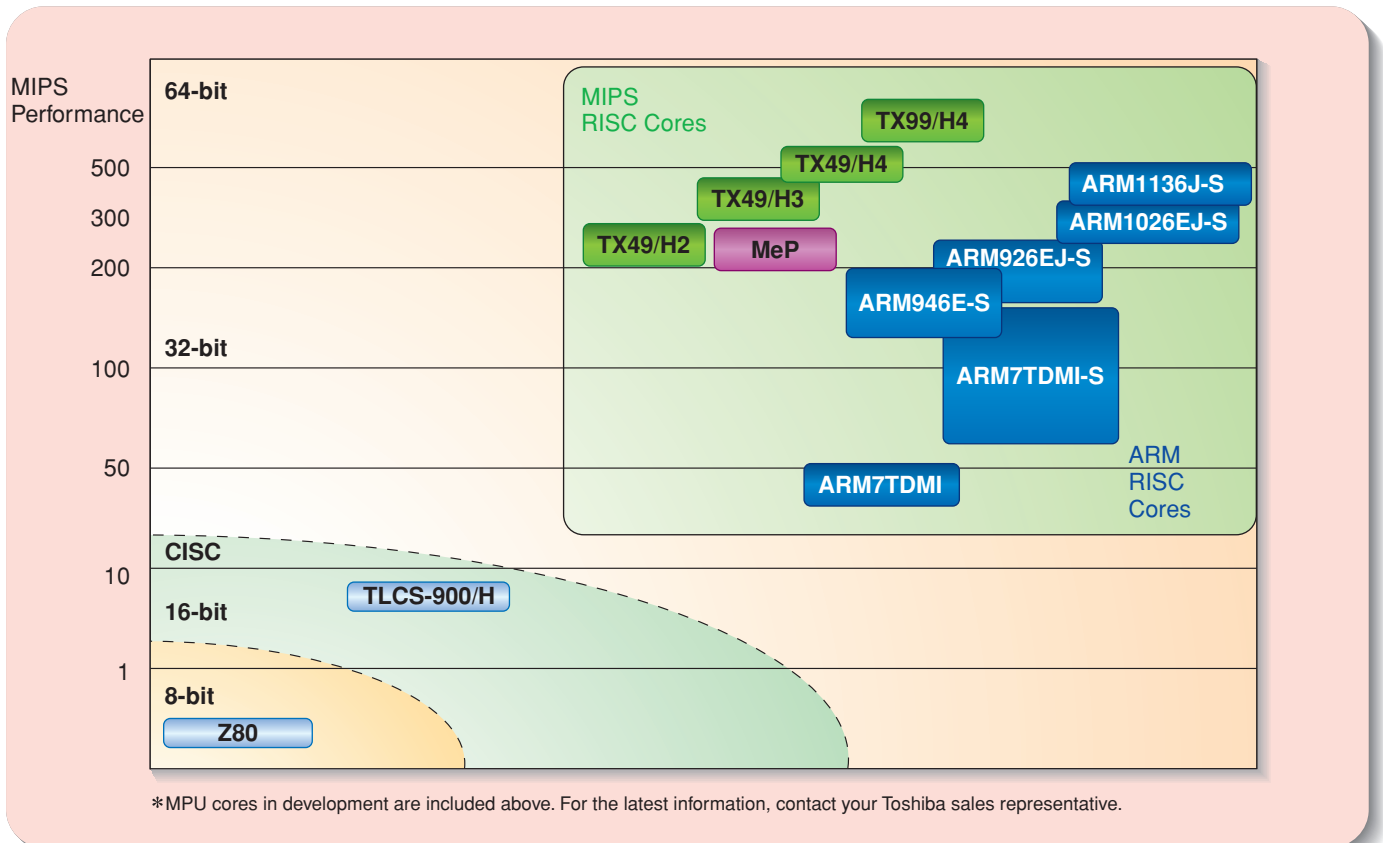
Megacells Targeted for System ASIC Applications

System ASIC Implementation

Toshiba offers a gallery of IP cores for system ASICs, including TX49 RISC cores, MeP cores, TLCS-900 CISC cores, DRAM cores and interface cores. Toshiba is also designing discrete components in such a manner as to make it easy to implement them as ASIC-ready IP cores.

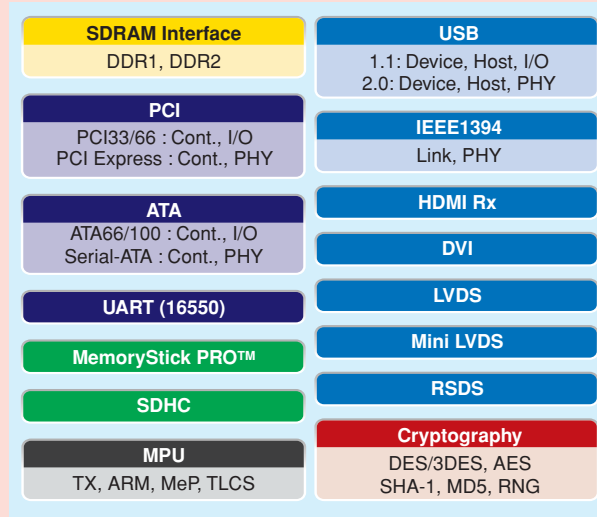


MPU Cores

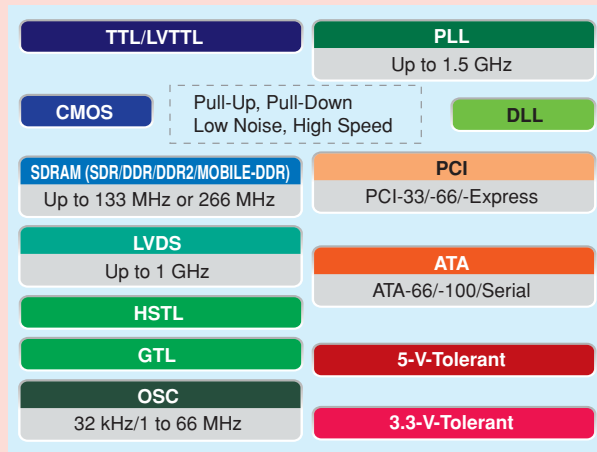


Cell Availability

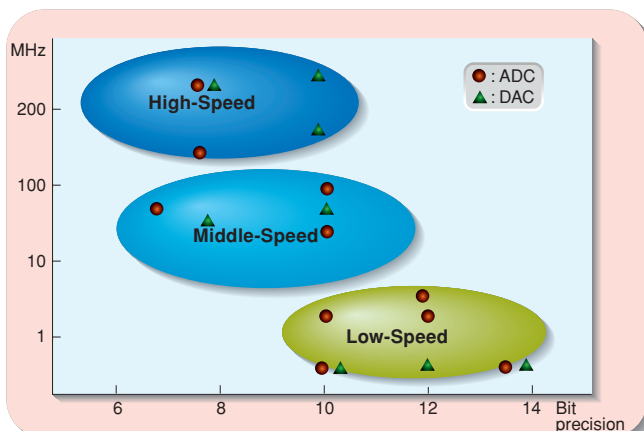
IP Cores



I/O Cells



A/D and D/A Converters



Memory (SRAM/ROM)

	RAM				Register File	ROM
	Async.	1-Port, Sync.	2-Port, Sync.			
TC190 (0.6 μm)	RAMA RAMC (~4kbits)	RAMB RAMC (~16kbits)	RAME RAMF RAMI		FV (1R/1W) FW (2R/1W) FX (2R/2W) FY (3R/1R)	ROMA ROMC ROMD
TC200 TC203 (0.4 μm)	RAMC (~4kbits)	RAML(~16kbits) RAMM(~128kbits)	RAMP (~64kbits)			ROMC ROMD
TC220 TC223 (0.3 μm)	High-Density, 1-Port	High-Density, 2-Port	High-Speed, 1-Port	High-Speed, 2-Port	Register File	ROM
TC260 (0.18 μm)	RAMS1D RAMS1F	RAMS2D RAMS2F	RAMS1E (~512kbits)	RAMS2E (~256kbits)	RFS11D (1W/1R) RFS12D (1W/2R) RFS14D (1W/4R) RFS22D (2W/2R)	ROMS1D (~1Mbits)
TC280 (0.13 μm)	RAMS1K (~512kbits) RAMS1J	RAMS2K (~256kbits) RAMS2J	RAMS1H (~512kbits)	RAMS2H (~256kbits)	RFS11G (1W/1R) RFS12G (1W/2R) RFS14G (1W/4R) RFS22G (2W/2R)	ROMS1G (~1Mbits)
TC300 (90 nm)	RAMS1L (~512kbits) RAMS1M	RAMS11M (~72kbits)	RAMS1V (~512kbits)	RAMS2V (~256kbits)	RFS11L (1W/1R) RFS12L (1W/2R)	ROMS1L (~1Mbits)

* A/D and D/A converters in development are included at left. For the latest information, contact your Toshiba sales representative.

Embedded DRAM Cores

With high memory data transfer rates and low power consumption, EDRAM SoCs enable high-performance and high-value-added systems. EDRAM SoCs also reduce system board area.

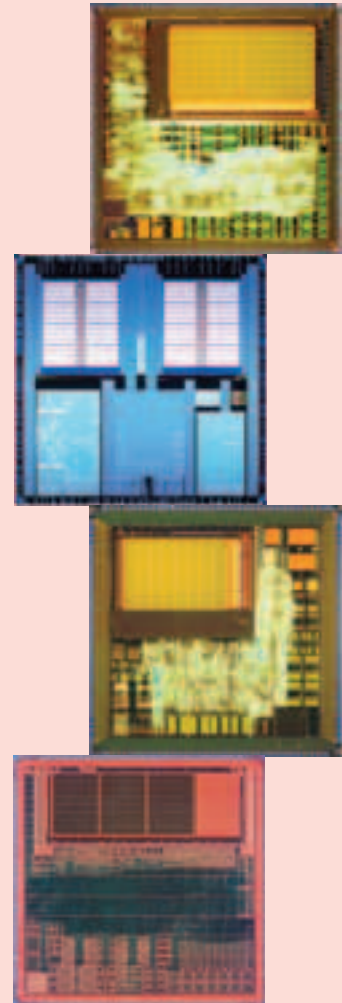
—SoCs with synchronous DRAMs and fast-access DRAMs

The ever-increasing design complexity and the drive for system-on-chips (SoCs) are driving demand for a greater capability to take advantage of pre-designed, re-usable building blocks. EDRAMs are one of the key components necessary for SoCs for the next-generation products. Through six generations of experience in EDRAMs, Toshiba has developed EDRAMs with differentiating data transfer rates and low power consumption.

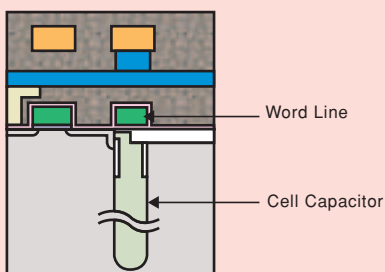
Toshiba's EDRAMs offer the following features and benefits:

- High performance with fast data transfer rates due to wide on-chip memory buses
- Much denser than SRAM
- Low power
- Soft error prevention
- System architecture optimization and reduction of discrete components
- Easy and effective testing with a direct-access test and DRAM BIST
- High yield through redundancy in DRAM macros
- Various types of DRAM macros with configurable depth and width

The low-power and high-bandwidth characteristics of Toshiba's embedded DRAM make it ideal for a wide range of applications, including video/image processing devices such as graphics and display controllers; storage devices such as HDD controllers; and digital communication and networking devices.



DRAM Core Features



Trench Process

The one-transistor (1T) DRAM cell structure utilizes the trench process. The trench capacitor allows for a planar surface topology that enhances reliability without compromising logic performance.

High Bandwidth

Freed from I/O restrictions, embedded DRAM cores provide high memory bandwidth with a synchronous interface and a bus width selectable from 64, 128 and 256 bits.

Configurable Macros

DRAM macros are configurable in depth and width to suit particular application requirements, allowing great system flexibility.

Low Power Consumption

DRAM macros consume less than 5% of power, compared to commodity DRAMs.

DRAM Cores for the TC300 Family

90 nm

The TC300C cell-based ASIC family, fabricated with drawn gate lengths of 65 nanometer offers a variety of embedded DRAM cores. Designers can use the same primitive and I/O cells as well as any IP cores available for the TC300C pure logic process without compromising logic performance.

The power-saving mode reduces the standby power of the DRAM cores, broadening the range of their applications in mobile equipment. The TC300C offers two types of DRAM cores.

Standard Synchronous DRAM (SD) macros

The standard SD macros are available in capacities from 2 Mb to 32 Mb and can operate over a wide range of clock frequencies. The SD macros are suitable for applications requiring fast page-mode accesses.

The Fast-Access (FA) DRAM macros offer significant advantages over the SD macros in random-access cycle times or data output times.

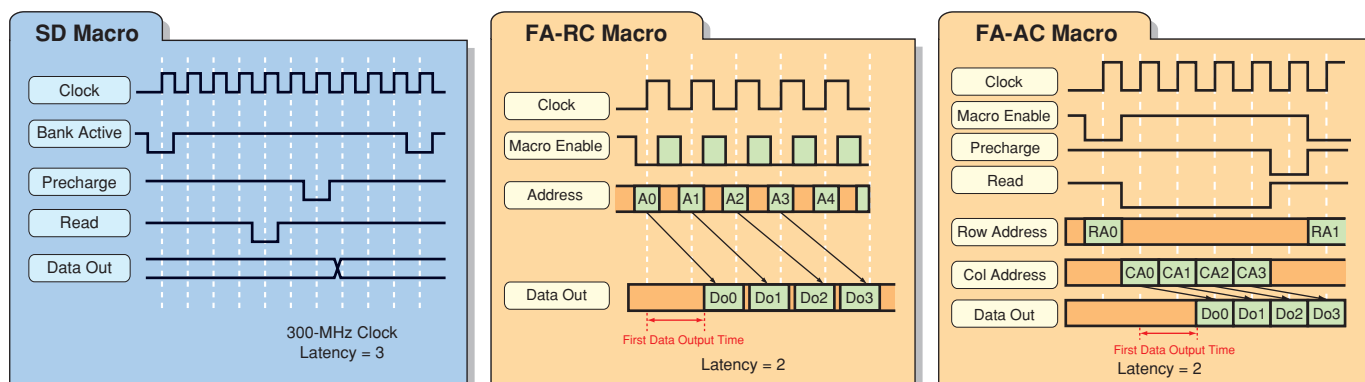
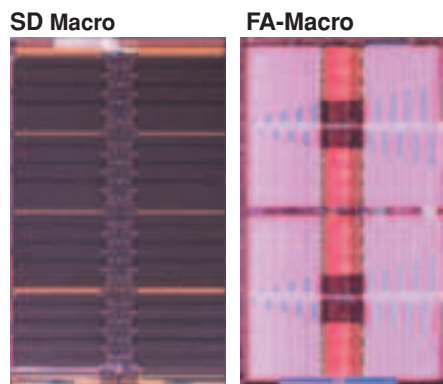
1. FA-RC macros have fast random-access cycle times

With random-access cycle times of 8 ns, the FA-RC macros are efficient for applications dominated by small random accesses.

2. FA-AC macros have fast 1st data output times

The FA-AC macros achieve an address-to-data-out delay as low as 6 ns for the first access.

These cores are ideal for applications requiring extremely fast page-mode accesses.



Characteristic	SD	SD(LP)*	FA-RC	FA-AC
Random Access Cycle Time	36 ns	40 ns	10 ns	10 ns
Latency	1, 2, 3	1, 2, 3	1, 2	1, 2
First Data Output Time			12 ns	6 ns
Max Clock Frequency (Page Mode)	300 MHz	200 MHz		300 MHz
Memory Capacity	2 to 32 Mb	2 to 32 Mb	2, 4, 8, 16 Mb	2, 4, 8, 16 Mb
Bit Width	64/128/256	64/128/256	32/64/128	32/64/128

*: The LP version consumes 1/10 the stand by current of standard SD macros.

DRAM Cores for the TC280 Family

0.13 μm

DRAM cores are also offered for use in ASICs based on the 0.11-micron drawn-gate-length TC280 family. SD and FA cores are available.

Characteristic	SD	FA-RC	FA-AC
Random Access Cycle Time	40 ns	10 ns	12 ns
Latency	1, 2, 3	1, 2	2
First Data Output Time		14 ns	10 ns
Max Clock Frequency (Page Mode)	250 MHz		250 MHz
Memory Capacity	2 to 32 Mb	2, 4, 8 Mb	2, 4, 8 Mb
Bit Width	64/128/256	128/256, 144/288	128/256, 144/288

● Product names or company names may be trademarks or registered trademarks of their respective owners.

ASIC Packaging

With increasing demands for higher system integration and single-chip implementation, semiconductor packages are not mere die housings any longer; they have become more of a crucial part of a system design. Toshiba offers a broad range of package options to satisfy all application needs, including system-in-packages (SiPs) specifically designed for high-end mobile devices and many other high-pin-count, small-form-factor and low-profile packages.

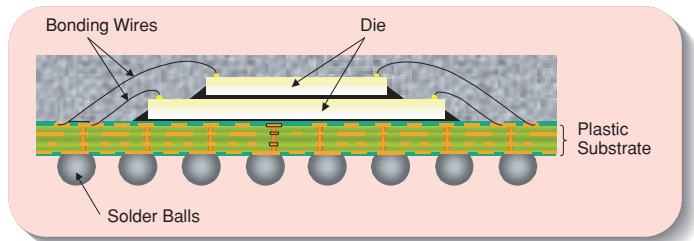
SiP Technology for Compact System Integration

The ever-evolving mobile devices have given rise to requirements for larger and higher-pin-count packages, and a greater number of chips. Now, we are confronted with two contradictory needs, high system performance and assize reduction. System-in-packages (SiPs) provide an ideal solution in such situations.

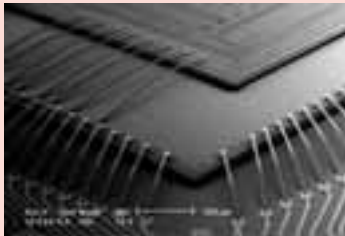
You can mix a variety of components such as logic and memory functions in a single package in side-by-side and stack-up configurations to save board space. BGA is the mainstay package style; all of the Toshiba's BGA packages, with the same ball counts and ball pitches, are available for SiP implementations.

Stacked PFBGA

PFBGA stands for "plastic fine-pitch ball grid array." Stacked PFBGAs allow multiple chips to be stacked on top of one another in a single package. The space-saving feature of stacked PFBGAs make them ideal for cell phone and mobile device applications. Stacked PFBGAs are available with the same ball counts and ball pitches as for standard PFBGAs.



Low-Loop wire Bonding and Backgrinding

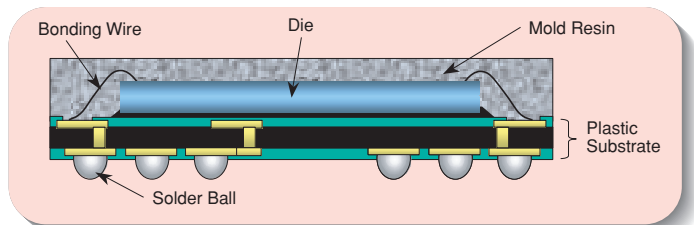


Package Height: 0.55 mm

PFBGA

PFBGA: Plastic Fine-Pitch Ball Grid Array

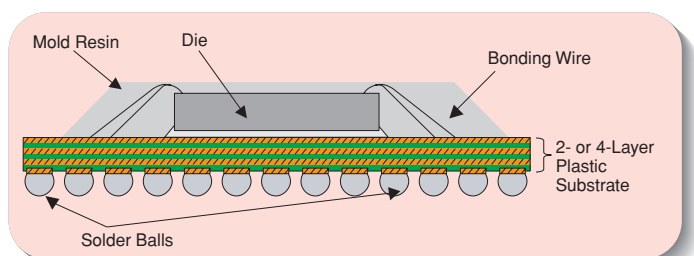
- Features: Small form factor and low profile
- Structure: The die is wire-bonded to a plastic substrate in an overmolded package body.
- Intended Use: PCs, DVD players/recorders, cell phones, etc.



PBGA/PBGA[4L]

PBGA: Plastic Ball Grid Array

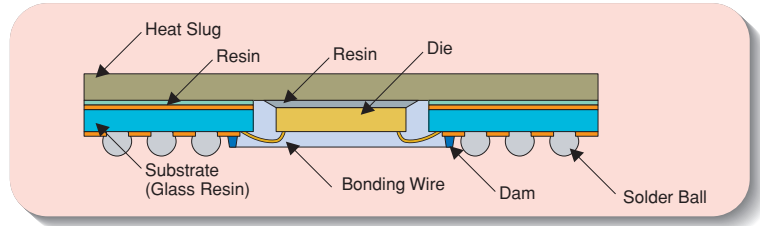
- Features: Small form factor and high pin count
- Structure: The die is wire-bonded to a plastic substrate in an overmolded package body.
- Intended Use: PCs, mobile devices, etc.



EBGA

EBGA: Enhanced Ball Grid Array

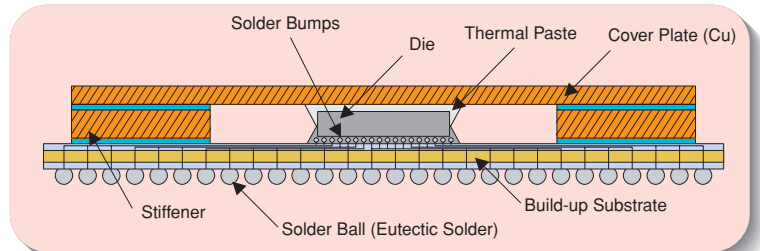
- Features: Enhanced thermal and electrical performance
- Structure: The die is directly attached, face down, to an integral heat sink.
- Intended Use: PCs, game consoles, etc.



PBGA[FC]

PBGA[FC]: Flip-Chip Plastic Ball Grid Array

- Features: High pin count (>1,000 pins)
- Structure: The die is flipped over so that solder bumps on the active surface of the die are soldered to the package substrate.
- Intended Use: Networking applications, etc.

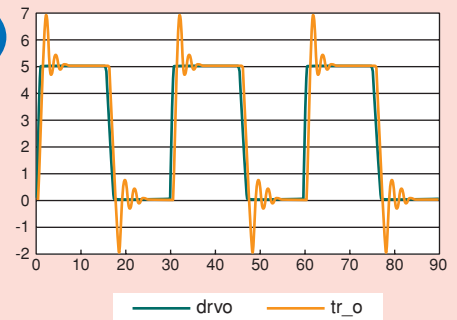
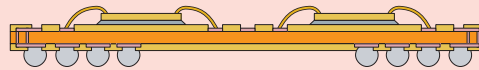


Development Support

- Electrical Simulation
Toshiba offers RLC extraction and HSPICE and IBIS modeling for electrical simulation.

High-Speed Interface
(ASIC-to-Memory)

RLC and SPICE
Models

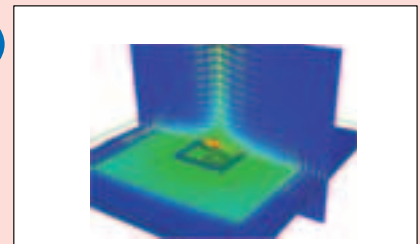


- Thermal Simulation
Toshiba offers package's thermal analysis, based on the package structure, chip size and substrate specifications.

High-Performance
High Power

Package
Design and
Materials

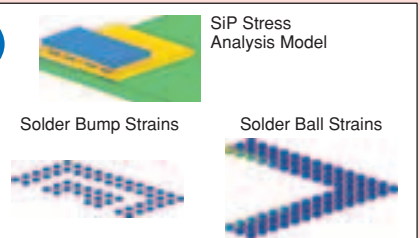
Temperature and airflow distribution in natural convection for a Side-by-Side SiP



- Stress Simulation
Toshiba provides analysis stress-induced strains in solder joints.

Low Profile
Stacked Die

Package
Structure and
Materials



ASIC Package Availability

Package Type	Pin Count Pin Pitch	Pin Count												
		100	200	300	400	500	600	700	800	900	1000	1500		
PBGA	1.27 mm			256	304	352	420	484	576					
	1.0 mm					352	420	500	560	648	768			
PFBGA	0.8 mm	97	121	141	145	177	217	265						
	0.65 mm		141	177	201	241	265	301	341	361	401			
	0.5 mm	97	145	169	193	217	241	265	289	313				
PQFP	1.0 mm	R64												
	0.8 mm	R80												
	0.65 mm	R100		160										
	0.5 mm				208									
LQFP	0.8 mm	44												
	0.5 mm	48	64	80	100	144	176	208						
	0.4 mm		128		176	216	256							
TQFP	0.5 mm	80	100											
	0.4 mm		128											
EBGA[4L]	1.27 mm				352		540							
PBGA[FC]	1.0 mm								625	841	1089	1444		

The above table includes packages being developed. For the latest availability status, contact your Toshiba sales representative. Toshiba also offers other packages not listed above. For details, contact your Toshiba sales representative.

The capability to deliver engineering samples at the earliest possible date

■ What is UniversalArray?

UniversalArray is a new type of cell-based IC platform for the deep-submicron and nanometer devices.

■ Overview

With SoC designs becoming larger and more complex, there is a growing need for a solution that helps reduce time-to-market and development cost. UniversalArray provides an ideal solution.

You can rely on UniversalArray to reduce time-to-market and development cost

- Design environment tailored to the state-of-the-art processes
Supports 130- and 90-nm technology nodes.
- Provides chip size and performance comparable to cell-based ICs.
- Uses the same cell library as for Toshiba's cell-based ICs.
- Achieves low power consumption comparable with cell-based ICs.

■ UniversalArray Solution

(1) Reduces the turnaround time of engineering samples

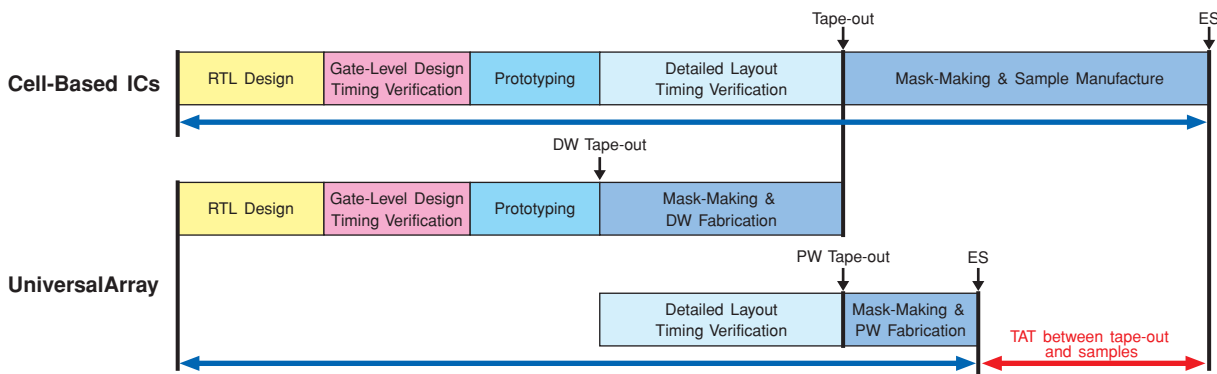
- With UniversalArray, diffused wafer (DW) fabrication starts before detailed layout of the logic portion of a chip is completed. This helps to reduce turnaround time between personalized wafer (PW) tape-out and the availability of engineering samples.

(2) Reduces the turnaround time of design spin-offs

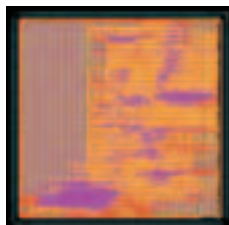
- With UniversalArray, the logic gate portion of a chip can be modified through only routing layers; even extensive ECO is possible. This helps to reduce the time required for mask tooling and chip manufacture.

(3) Reduces cost for design spin-offs

- UniversalArray reduces the number of masks required for design spin-offs, cutting the rework cost.

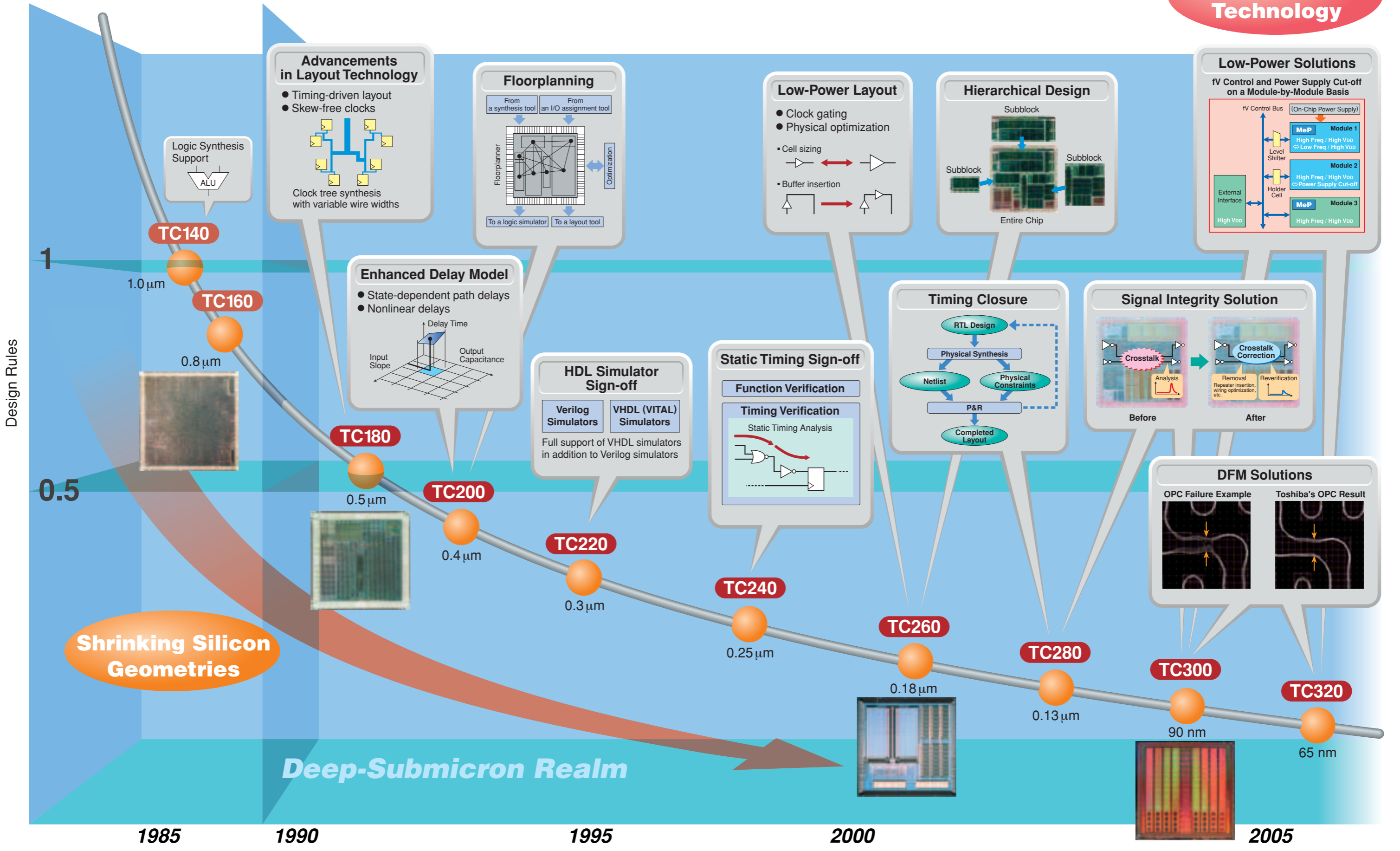


Chip Layout Example



— General Specification —

- Application: Cell phones
- Technology: **TC280** (130 nm)
- Logic: Approx. 2 MGates
- Memory: 8Mbit DRAM
132 SRAMs



Design Rules

1

0.5

Shrinking Silicon Geometries

Deep-Submicron Realm

1985

1990

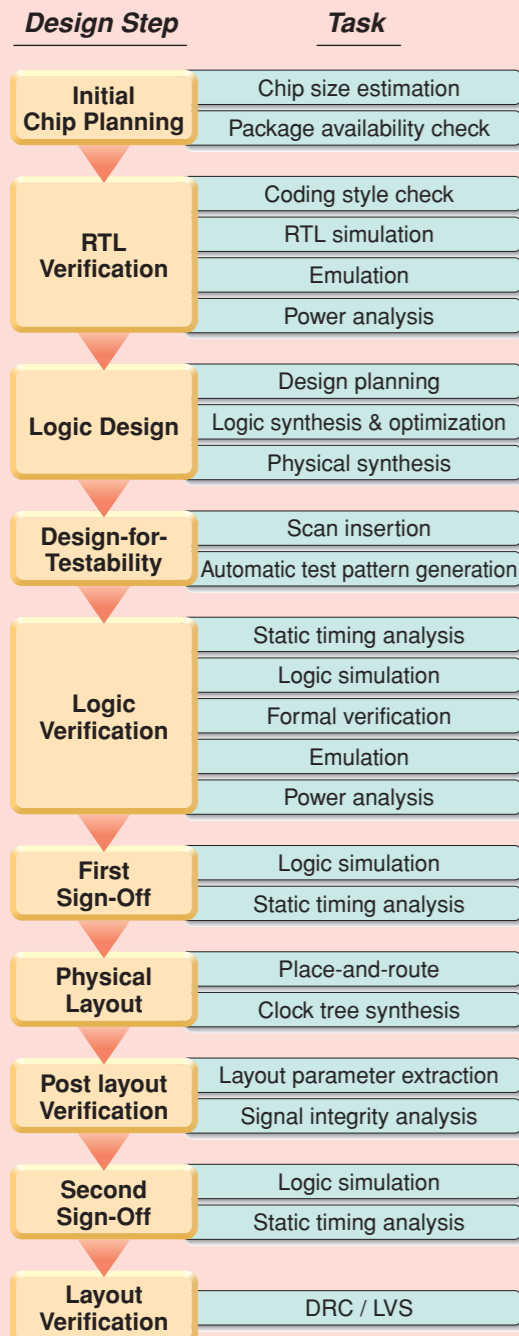
1995

2000

2005

Design Kit Support

Typical Design Flow



Supported EDA Tools and Design Kit Availability

ASIC Product Family		Cell-Based ICs										Universal Arrays		Gate Arrays					Embedded Arrays						
		TC 320C	TC 300C	TC 280C	TC 260C	TC 223C	TC 222C	TC 220C	TC 203C	TC 200C	TC 190C	TC 300	TC 280	TC 223G	TC 220G	TC 203G	TC 200G	TC 190G	TC 260E	TC 223E	TC 220E	TC 203E	TC 200E		
EDA Tool	Logic Synthesis Tools	Design Compiler	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
	Verilog-XL	—	—	—	—	●	●	●	●	●	●	—	—	●	●	●	●	●	—	●	●	●	●	●	
Simulators	VCS	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	NC-Verilog	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	NC-Sim	●*1	●*1	●	●	●	●	●	●	●	●	●*1	●	●	●	●	●	●	●	●	●	●	●	●	
	ModelSim	●*1	●*1	●	●	●	●	●	●	●	●	●*1	●	●	●	●	●	●	●	●	●	●	●	●	
	NC-VHDL	—	—	●	●	●	●	●	●	●	●	—	●	●	●	●	●	●	●	●	●	●	●	●	
	Static Timing Analysis Tools	PrimeTime	●	●	●	●	●*2	●*2	●*2	●*2	●*2	●*2	●	●	●*2	●*2	●*2	●*2	●*2	●	●	●	●	●	●
Formal Verification Tools	Formality	●	●	●	●	—	—	—	—	—	—	●	●	—	—	—	—	—	●	—	—	—	—	—	
	Conformal LEC	●	●	●	●	—	—	—	—	—	—	●	●	—	—	—	—	—	●	—	—	—	—	—	
DFT Tools	DFT Compiler / BSD Compiler	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	DFTAdvisor / FastScan	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	TetraMAX	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
Power Analysis and Optimization	PowerTheater	●	●	●	●	—	—	—	—	—	—	●	●	—	—	—	—	—	●	—	—	—	—	—	
	Power Compiler	—	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
Emulators	Palladium II	●	●	●*3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		

The above table shows the basic cell availability status. For availability of megacells such as RAMs and ROMs, ask the nearest Toshiba ASIC design center. Please obtain the latest technical material before you begin creating a design.

- *1: The ModelSim and NC-Sim libraries for the TC300C series support only Verilog HDL.
- *2: Not supported for timing sign-off using PrimeTime
- *3: Supported with libraries designed for Celaro, an emulator previous to Palladium II.

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Toshiba ASIC Product Lines

Cell-Based ICs

The cell-based technique assembles pre-designed and pre-optimized cells that users select, place, and interconnect on-chip to produce the required circuit functions with optimum chip size. Because all of the mask set needs defining, the lead times to prototypes and production is longer than for a gate array. However, cell-based ICs provide greater design flexibility, making them ideally suited for increased system integration and aggressive performance targets. Therefore, a library of a wide variety of cells is essential to the success of cell-based designs. Toshiba offers various types of memory, CPU peripherals, analog cells and many others.

Product		I/O: Mixed 2.5/3.3 V			I/O: 3.3 V		I/O: 5 V	I/O: Mixed 3.3/5 V	
		Core: 1.2 V	Core: 1.5 V		Core: 3.3 V		Core: 5 V	Core: 3.3 V	
		TC300C	TC280C	TC260C	TC220C	TC200C	TC190C	TC223C	TC203C
Process		90 nm	0.13 μm	0.18 μm	0.3 μm	0.4 μm	0.6 μm	0.3 μm	0.4 μm
Gate* Delay	Fanout = 1	14 ps	28 ps	47 ps	0.06 ns	0.10 ns	0.12 ns	0.06 ns	0.10 ns
Gates (Usable)		—	—	16.7 M	2.1 M	538 k	538 k	2.1 M	718 k
Gate Density		403 kG/mm ²	206 kG/mm ²	125 kG/mm ²	—	—	—	—	—
Pads	Wide Pitch	—	—	652	512	432	432	504	504
	Narrow Pitch	—	—	1028	1028	868	868	1028	1028
Power**	Fanout = 1	0.00867	0.0127	0.0193	0.24	0.48	0.94	0.24	0.48
Masterslice		Fabricated for each design	Fabricated for each design	120	40	39	39	40	38

* 2-input NAND, X2 ** $\mu\text{W}/\text{gate}/\text{MHz}$ 2-input NAND, XL

Embedded Arrays

Embedded arrays combine high-performance functions of cell-based ICs with the gate array advantage of quick turnaround. Embedded arrays use the same sea-of-gates technology as gate arrays, but allow designers to "embed" dense hardmacrocells and compilable cells in a gate array base by replacing part of its sea-of-gates core area with cell-based versions of the blocks.

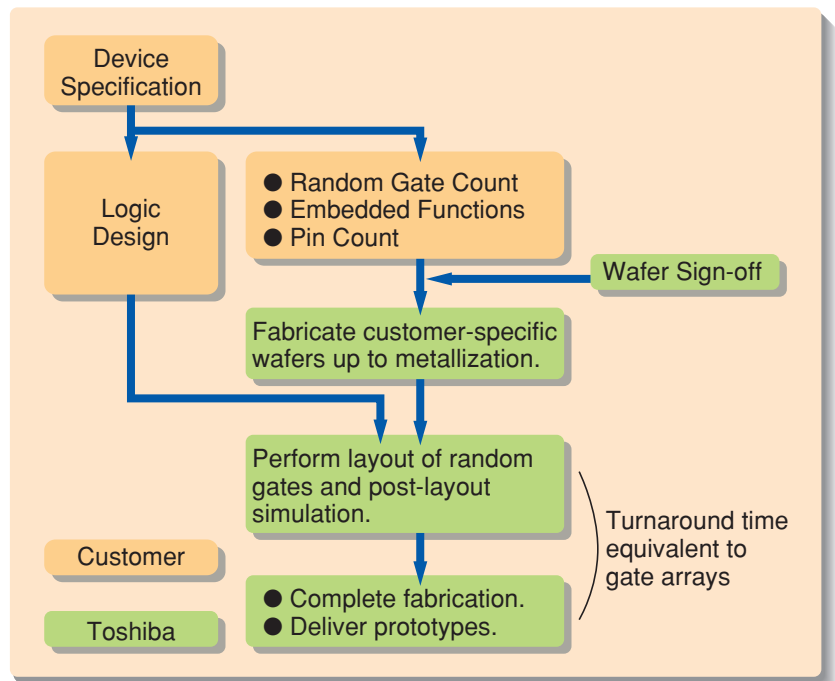
Product		I/O: Mixed 2.5/3.3 V Core: 1.5 V	I/O: 3.3 V Core: 3.3 V		I/O: Mixed 3.3/5 V Core: 3.3 V	
		TC260E	TC220E	TC200E	TC223E	TC203E
Process		0.18 μm (Ldrawn = 0.14 μm)	0.3 μm	0.4 μm	0.3 μm	0.4 μm
Delay*	Fanout = 1	0.05 ns	0.07 ns	0.11 ns	0.07 ns	0.11 ns
	Fanout = 2 + wiring	0.06 ns	0.15 ns	0.19 ns	0.15 ns	0.19 ns
Gates (Usable)		9.3 M	1.9 M	503 k	1.9 M	694 k
Gates Density		65kG/mm ²	—	—	—	—
Pads	Wide Pitch	652	512	432	504	504
	Narrow Pitch	1028	1028	876	1028	1028
Power**		0.036 μW	0.65 μW	1.14 μW	0.65 μW	1.14 μW
Masterslice		120	38	39	40	38

* High-drive 2-input NAND gate, ** $\mu\text{W}/\text{gate}/\text{MHz}$, 2-input NAND, fanout = 1

The figure at right illustrates the embedded array design flow.

Early in the design cycle, the customer determines the appropriate area of logic gates, functions to be embedded, and the number of I/Os required. The customer then continues development work while Toshiba fabricates customer-specific base arrays (or master wafers). Once the customer completes the design, the layout of the gate array portion of the design is performed on the inventoried customer-specific master wafers. Post-layout simulation is then performed to verify that the design works to specifications. On customer approval of the design, prototype production can begin with the pre-defined master wafers already waiting at the metal mask step.

Toshiba personalizes the master wafers by the use of up to six layers of metallization in much the same way as—and as quickly as—a gate array. As such, if any design re-spins are necessary, they can be produced with the gate array lead times.



Gate Arrays

A gate array consists of a matrix of transistors in a sea-of-gates architecture that are diffused into silicon called masterslices. These masterslices are personalized at the metal wiring stage by applying a unique interconnection pattern that implements the customer's logic design. Therefore, development time is short. Toshiba's gate arrays offer single gate array solutions for a wide variety of digital logic applications ranging in size from 300 to 1.9-M gates.

Product	I/O: 3.3 V Core: 3.3 V		I/O: 5 V Core: 5 V	I/O: Mixed 3.3/5 V Core: 3.3 V	
	TC220G	TC200G	TC190G	TC223G	TC203G
Process	0.3 μm	0.4 μm	0.6 μm	0.3 μm	0.4 μm
Delay*	Fanout = 1	0.07 ns	0.11 ns	0.07 ns	0.11 ns
	Fanout = 2 + wiring	0.15 ns	0.19 ns	0.24 ns	0.15 ns
Gates (Usable)	1.9 M	704 k	704 k	1.9 M	694 k
Pads	Wide Pitch	512	512	504	504
	Narrow Pitch	1028	1036	1036	1028
Power**	0.65 μW	1.14 μW	2.46 μW	0.65 μW	1.14 μW
Masterslice	24	28	28	24	26

* High-drive 2-input NAND gate, **μW/gate/MHz, 2-input NAND, fanout=1

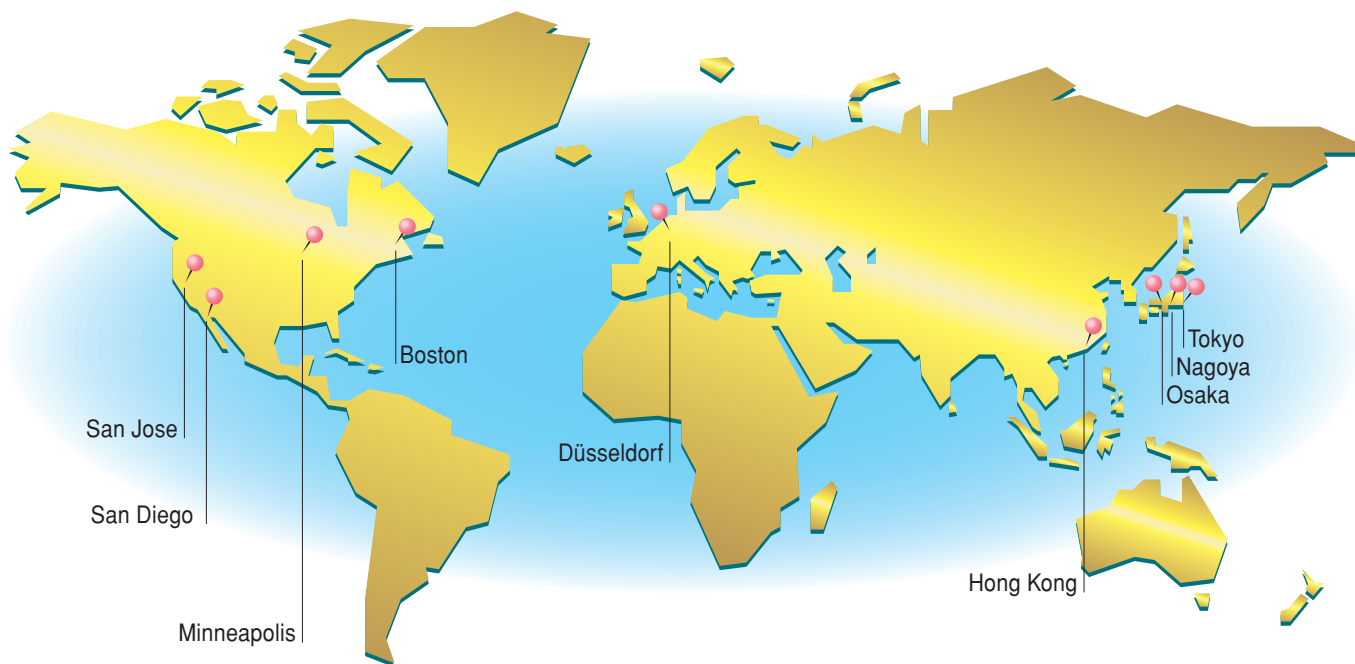
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Support and technical excellence are the areas that are given the highest priority at Toshiba. Toshiba ASIC Design Centers are located around the globe and provide a high level of technical expertise for support before, during, and after the design of a Toshiba ASIC. This includes support issues dealing with EDA environments and design kits, Toshiba design methodologies, Toshiba ASIC technologies, and Toshiba ASIC design implementation. They are also available for design consultation.

A worldwide commitment to excellence

Toshiba has built a reputation around the world for delivering high-performance, trouble-free products at competitive prices. This reputation is no accident. It stems from a corporate culture dedicated to excellence in product design, processes, high-volume manufacturing techniques, and quality assurance at every stage of production. Excellence is also the result of a commitment to service anywhere in

the world, before, during, and after the design. This not only means that Toshiba application engineers work with customers to develop the best and most cost-effective product for each individual application. It also means that products are delivered as specified and that we constantly get feedback from customers about how we can better meet their needs. Toshiba's company-wide and worldwide commitment to excellence is just one more reason to choose Toshiba as your ASIC partner.



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