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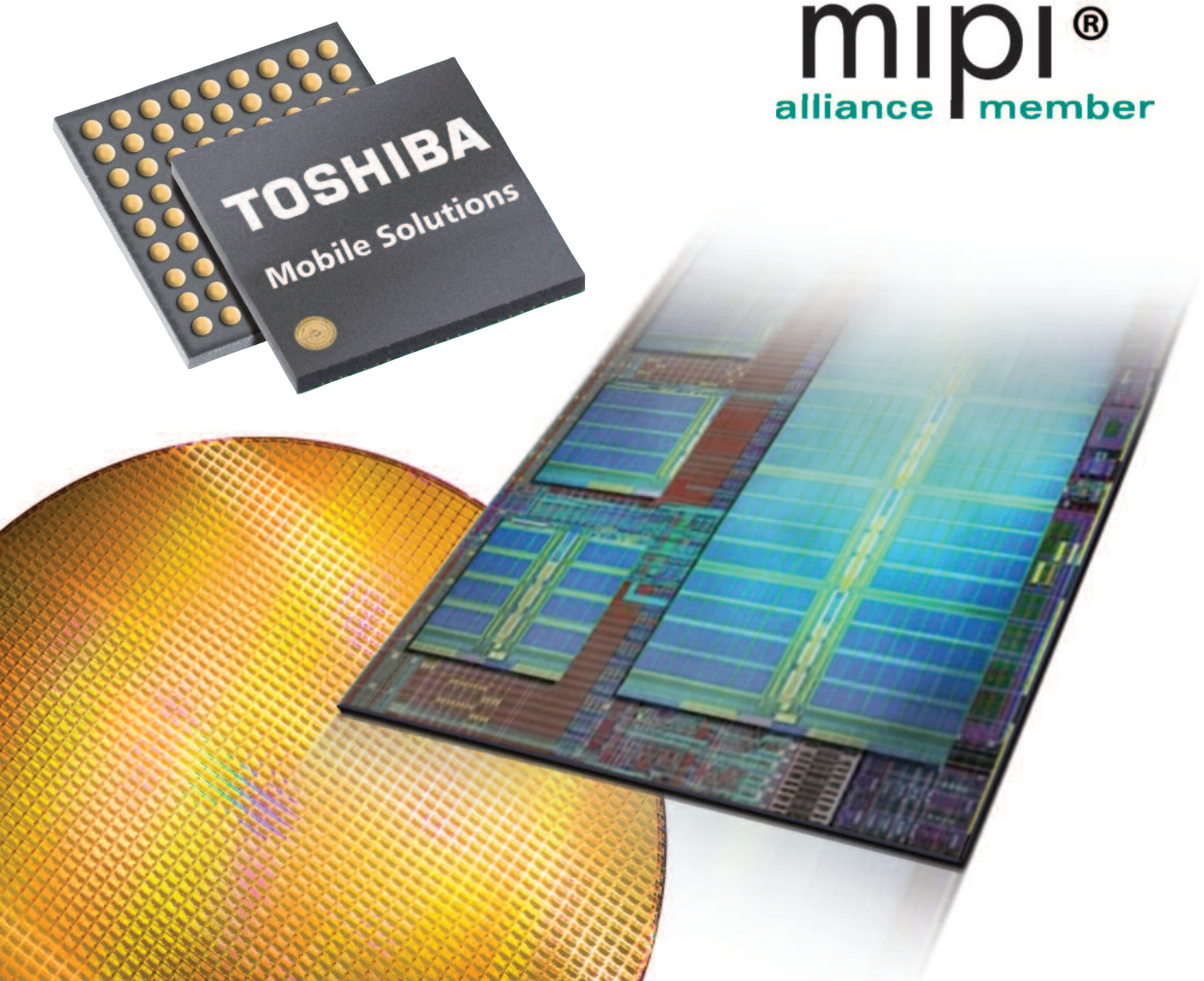
TECHNOLOGIES FOR MIPI®

COMPLETE MIPI SOLUTIONS FROM TOSHIBA

mipi® alliance member



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THE MOBILE INDUSTRY PROCESSOR INTERFACE (MIPI®) ALLIANCE

Consumer demand to access ever more advanced applications and high levels of multimedia content from personal and portable devices is driving the need for the underlying system architectures to evolve rapidly.

Modern processors or system-on-chip (SoC) devices typically have several ports or busses which interface to a variety of peripherals such as displays, cameras, memory, or communications devices. There may also be interconnections among the peripheral devices themselves. As a result, new and emerging mobile applications require integrated SoC solutions that deliver high bandwidth interface capabilities.

The Mobile Industry Processor Interface (MIPI®) Alliance is an open membership organization incorporating leading companies in the mobile industry that share the objective of creating and promoting open standards for interfaces to mobile application processors. By defining such standards and encouraging their adoption throughout the industry value chain, the MIPI Alliance intends to reduce fragmentation and improve interoperability among system components, benefiting the entire mobile industry.

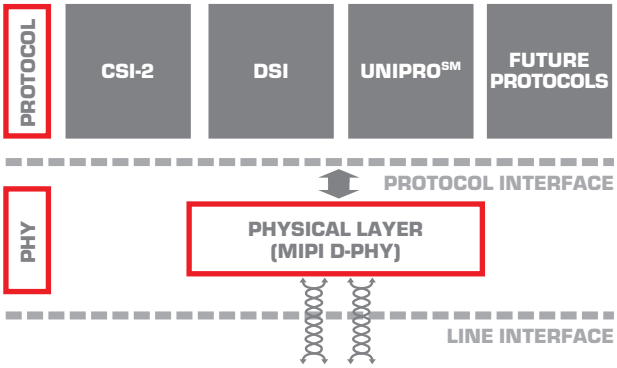
TOSHIBA AND MIPI

Toshiba has been a MIPI Alliance member since 2004. Since then, the company has developed technologies and in-house expertise that provides customers with complete MIPI-compliant solutions encompassing both the physical layer and the various MIPI protocols.

Toshiba has already demonstrated its ability to deliver MIPI-compliant technologies in a number of customer designs as well as its own application specific standard products (ASSPs). Based on the company's advanced 90nm, 65nm and 40nm CMOS ASIC technologies, Toshiba MIPI-compliant ASSPs include devices for display sub-systems as well as camera applications.

COMPLETE MIPI SOLUTIONS

Toshiba provides both physical layer and protocols that support the rapid development of complete MIPI-compliant transmit and receive solutions.



Toshiba's MIPI offering includes

D-PHY
A scalable, bi-directional, low-power, high-speed physical layer upon which several MIPI interface standards are based (see below). The same D-PHY can be used for hi-speed serial communications in high speed mode and with single-ended transmission lines in low power mode. This makes it ideal for implementing a variety of different applications, including next-generation camera designs and high-speed display communications.

CSI-2 (CAMERA SERIAL INTERFACE 2)
Based on D-PHY, CSI-2 provides the interface between a camera module and, for example, the system host. The low pin count of CSI-2 enables camera signals to be carried across the limited conductors in the flex circuits of flip phone hinges. A total data rate of the link as high as 4Gbps enables new camera features and support sensor resolutions beyond 10Mpixel.

DSI (DISPLAY SERIAL INTERFACE)
Building on the core advantages of the D-PHY technology, DSI is a higher layer protocol with error correction that provides solutions for display-related data communication. DSI supports both "smart" (buffered) and "video mode" (unbuffered) display panels. The MIPI Alliance has specified a specific DCS (display command set) that sits above the DSI and defines a standard software interface for different suppliers.

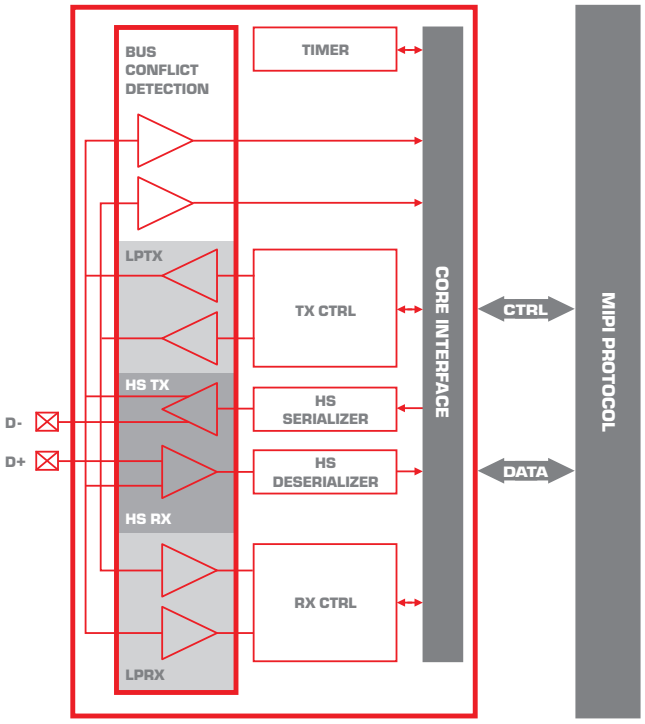
UNIPRO℠ (UNIFIED PROTOCOL)
UniPro℠ is PHY-independent and provides a single, unified reliable protocol that can be used across several applications including cameras, displays and device communication interfaces. UniPro℠ offers high-speed communications, error correction for reliability, and low energy per transferred bit. Currently UniPro℠ provides point-to-point functionality, but future generations will support network capabilities. Fully compatible with the existing D-PHY, UniPro℠ will also support future, higher speed M-PHY implementations.

FUTURE PROTOCOLS – Toshiba will continue to develop solutions for future MIPI protocols as they become available.

ADDITIONAL IP – Toshiba also offers a variety of additional IP in support of MIPI solutions, including optional PLL IP, lane control and interface logic.

MIPI D-PHY MODULE

At the heart of Toshiba's MIPI solution is the MIPI D-PHY module.



This PHY is compliant with the MIPI D-PHY specification and provides a re-usable physical layer solution with support for one to four data channels and a single clock channel. MIPI camera interfaces (CSI-2), display interfaces (DSI) and Unified Protocol (UniPro℠ 1.0/1.1) are based on the MIPI D-PHY.

In High Speed (HS) mode the MIPI D-PHY can deliver from 80Mbps up to 1Gbps per lane (depending on implementation and technology) via an advanced source-synchronous, differential SLVS transceiver which is scalable to the number of lanes required by the application.

In Low Power (LP) mode the D-PHY offers single-ended transmission speeds up to 10Mbps. Depending on the application operational power is in the mW range and standby power is in the µW range.

D-PHY meets the requirements of low-power, low emission, and high-noise immunity that mobile phone designs demand. Based on 1.2V supplies, it scales well across future semiconductor process technologies.

MINIMUM CONFIGURATION		4 wires only unidirectional or half-duplex
MAXIMAL CONFIGURATION		10 wires
MEDIUM		<30 cm PCB, flex, micro coax
DATA RATE PER LANE	**HS** **LP**	>80 Mb/s - up to 1Gb/s <10 Mb/s
ELECTRICAL SIGNALING	**HS** **LP**	SLVS-200 LVCMOS1.2V
HS CLOCKING METHOD		DDR Source-Sync CLK
HS LINE CODING		None or 8b9b
RECEIVER CDR REQUIRED		No

SILICON-PROVEN SOLUTIONS

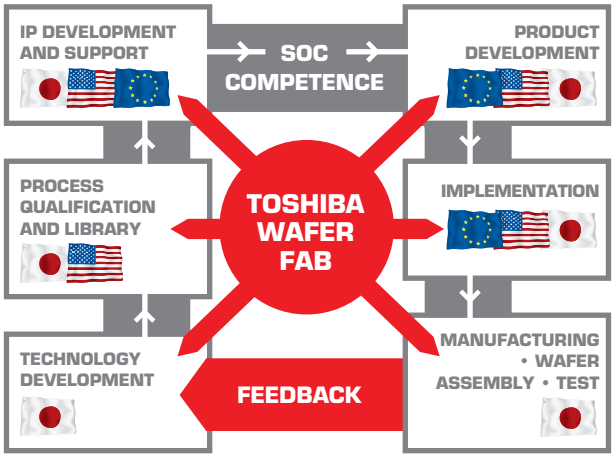
When choosing MIPI solutions from Toshiba customers have the additional benefit that the technologies have already been silicon-proven in Toshiba's own ASSPs. Based around the MIPI D-PHY Toshiba has developed products for display control and, using its leadership in the field of CMOS image sensors, CSI-2-based camera modules.

Take, for example, the TC358731XBG enhanced MIPI display buffer/controller.

The TC358731XBG is designed to reduce the total system power consumption when large size mobile displays have to be driven. Features include 8Mbit of embedded DRAM (eDRAM) to provide flexible image buffering for displays with up to VGA resolution.

DEVELOPING MIPI-BASED SOCS – THE IDM MODEL

With Toshiba, developing MIPI-based SOC solutions could not be easier. Unlike third party design houses, Toshiba's Integrated Device Manufacturer (IDM) model allows the company to provide total SoC competence. As a result, customers deal with a single organisation from initial IP sourcing to design, through testing, and on into final manufacture.



As an IDM, Toshiba's intimate involvement with the underlying process technology and rapid access to production feedback ensures that designs can be optimised and customised with final production in mind from the very beginning of the development process. This includes verifying and testing of IP in the customer product.

For the customer, the IDM model also eliminates the blurring of the boundaries of responsibility. Toshiba's responsibility encompasses everything from IP to final production and yield optimisation, providing the peace of mind that customers are working with a company that shares their objective of delivering successful volume silicon with the shortest possible turn-around-time (TAT).

SUPPORTING SOC IMPLEMENTATION

To speed and simplify the implementation of SoCs based on the company's advanced CMOS processes, Toshiba offers a variety of development handover models including:

ASIC MODEL

- RTL handover with synthesis, place-and-route, and verification by Toshiba or gate-level handover with synthesis by customer and layout implementation by Toshiba

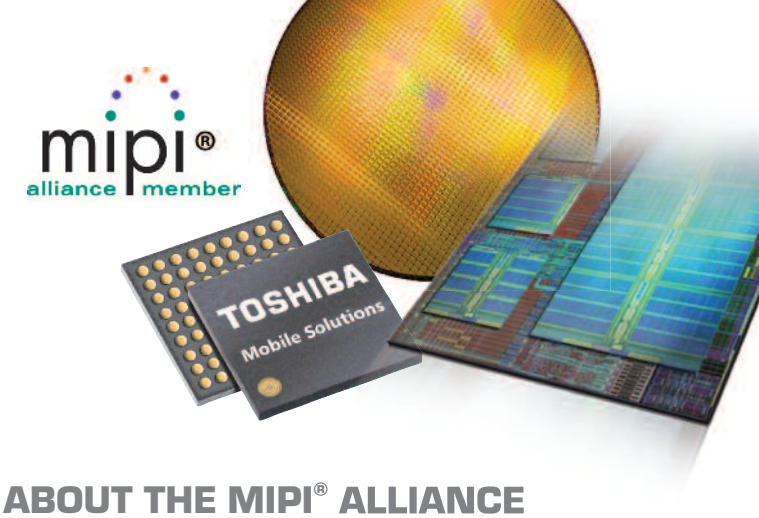
SEAMLESS "HYBRID" MODELS

- Mixed-signal IP/block development by customer based on PDK, and chip-level integration by Toshiba (RTL handover or gate-level handover)

FULL COT (CUSTOMER OWN TOOLING) MODEL

- Physical data handover (GDSII) by customer.

In each handover model, engineers at Toshiba's local European LSI Design and Engineering Center (ELDEC) are available to provide full technical support, advice and guidance relating to the integration-, QA- and testing of the mixed-signal IP.



ABOUT THE MIPI® ALLIANCE

The MIPI Alliance is a non-profit corporation that operates as an open membership organization. All companies in the mobile industry are encouraged to join, including handset manufacturers, semiconductor companies, hardware peripheral manufacturers, and operating system vendors. More than 160 member companies actively participate in the Alliance.

For more information on the MIPI Alliance visit: www.mipi.org

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